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Grid-Connected Inverter Output Impedance Reshaping for Passivity Enhancement and Disturbance Rejection

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ABSTRACT To improve both the stability and the disturbance suppression ability of single-phase grid-connected inverters through LCL filters, this paper proposes an inverter output impedance enhancing control mechanism. The impedance enhancing control mechanism employs a virtual impedance control and a node-voltage feedforward control to ensure sufficient passivity and high amplitude of inverter output impedance over wide frequency range of interest. The proposed control mechanism is realized through combination control of a low-voltage bidirectional voltage-source-converter (B-VSC) connected at the filter capacitor branch and the main inverter. The B-VSC sustains an extra low power without sacrificing the efficiency of the inverter. Both the simulation and experimental results are finally given to verify the validity of the proposed method, which shows the performance improvement of the proposed radial-line inverter system working under variable grid conditions.

INDEX TERMS Inverters, stability, passivity, impedance enhancement.

I. INTRODUCTION

Distributed renewable energy resources access to the power grid through the radial-line configuration [1], as illustrated in Fig. 1(a), where distributed photovoltaic (PV) inverters are often equipped with high-order harmonic filters, such as LCL or LLCL filters [2], [3]. Due to the local filter resonance, dynamic interactions, or harmonic disturbances at the point-of-common-coupling (PCC), instability or resonance problems of the distributed power systems may be caused.

Many previous efforts have been devoted to study the stability, dynamic interactions, and current circulation among paralleled inverters in proximity or at the same PCC [4]–[11]. Particularly, previous work in [4] and [5] has already shown that multiple distributed inverters with high-order power filters could also exhibit multiple resonances. Inherent resonance induced by local filter, parallel resonance among inverters and series resonance between inverters and the grid all together form the multiple resonances. Therefore, the distributed power generation system (DPGS) may be affected by local filter resonance, multiple interactive resonance, and grid disturbances. Even when single inverter is designed to suppress the local filter resonance and ensure the inverter stability [12]–[14], multiple paralleled inverters still face the challenge of harmonic interactions. The impedance stability analysis method has been established to evaluate such harmonic stability problem [15], [16]. As studied in [8], if all distributed power generation (DPG) inverters together with control are assumed to be identical, the impedance-based stability criterion will incorporate DPG inverters into a single unit. Then, mathematical results show that the equivalent grid impedance is amplified N times in terms of a single inverter. This analysis explains why multiple paralleled inverters can still become unstable even if all single inverters are designed stably. To further investigate the generic characteristics of parallel operation, the system transfer function matrix with no hypothesis of identical inverters is also derived in [8], which
is followed by some interesting research work [4]–[6], [11]. They focus on studying the harmonic interactions between paralleled inverters and the grid.

The impedance-model representation of the radial-line renewable system with dominant distributed feeder impedance is shown in Fig. 1(b). Because each inverter in radial-line system is installed at different positions on the grid, the interactions between each inverter and the grid are different with each other [1], [17]–[22]. The impedance-based stability criterion cannot merge them into a single unit even with identical inverters. Thus, the generalized Nyquist criterion (GNC) is adopted to examine both the right-half-plane (RHP) poles of the complicated return-ratio matrix and the encirclement of the Nyquist plot around \((-1, j0)\) [23]. In [18] and [21], the impedance model is used to predict the stability of each inverter through the impedance ratio between the inverter output impedance and the equivalent impedance of the rest system. The method in [22] develops an impedance-based sufficient stability criterion by checking the characteristic loci of the return ratio matrix at each bus. If the number of multiple inverters is large, the calculation of each return ratio matrix is complicated. In that case, it is difficult to make a complete assessment of the system characteristics. To solve the abovementioned problems, a popular technique is developed by the passivity concept: all connected sub-systems must be passive for the DPGS to be stable [9], [24]–[27]. Passivity-based stability criterion provides controller design rule for each inverter to act passively over wide frequency range and ensures the system stability regardless of the grid impedance [28]. However, the digital delay in digitally-controlled inverters arouse the adverse impact on the passivity of single inverter because it could bring in RHP poles in the transfer functions [29], [30]. Many robust control methods have been proposed to solve the problems caused by the digital delay. For example, robust active damping methods aim to broaden the range of positive virtual resistance mainly by reducing the computation delay [30] or adopting hybrid damping schemes [31], [12], and phase-compensated resonant controller improves the inverter stability by carefully adding a phase leading angle at the resonant frequency [32], [33]. However, these methods mainly focus on improving the inverter stability. With the increase of grid impedance, the influence of abundant grid background harmonics on the inverter output current cannot be ignored. Generally, there are two kinds of control methods to suppress the grid disturbances. One is by improving the open-loop gain at the frequencies of grid background harmonics, such as multi-resonant controller. The other is using the feedforward mechanism of PCC voltage. However, the feedforward control will weaken the system stability in the weak grid [34], [45]. Adaptive and robust PCC voltage feedforward improves the disturbance suppression capability of the inverter even under the weak grid by using multiple band-pass filters (MBPF) or relying on the grid impedance estimation algorithm [35], [36]. The demerit of the MBPF-based PCC voltage feedforward or the multi-resonant controller is that it lacks the ability to suppress non-characteristic harmonics, such as the interactive harmonics between multiple inverters and the grid.

To ease such concerns, inserting a shunted or series active damper at the PCC can effectively emulate the positive resistor [37]–[40], which helps the system viewed at the PCC be passive and immune to grid background harmonics. However, the common current injected to the grid does not include the circulating current information between inverters [5], [41]. Namely, the active damper at the PCC cannot suppress the circulating current resonance between inverters.

From this perspective, this paper attempts to find a local way to increase the inverter output impedance and guarantee the passivity of all connected inverters. Thus, an inverter output impedance enhancing control mechanism is proposed, which is capable of guaranteeing sufficient passivity and strong resistance to grid disturbances of each inverter in the DPGS, improving the grid current quality in the case of wide grid impedance variation. The main contributions of this paper can be summarized as follows.

1) An inverter output impedance enhancing control method is proposed, which guarantees sufficient passivity and strong resistance to grid disturbances of each inverter in the DPGS.

2) A low-voltage bidirectional voltage-source-converter (B-VSC) connected at the filter capacitor branch is proposed to help achieve passivity control and impedance
enhancement, and the corresponding control scheme is also provided.

3) The design principles of the control parameters in the proposed method are deduced successively.

The rest of this paper is structured as follows. First, according to the impedance-based modeling in Sec. II, the inverter output impedance enhancement aiming at improving the system stability and resistance to grid disturbances can be deduced. Then, the configuration of the radial-line inverter system equipped with the proposed impedance enhancing control mechanism is presented in Sec. III. Modeling analysis and simulation results with a 16-paralleled radial-line inverter system is followed in Sec. IV and V. In Sec. VI, experimental setup with a 3-paralleled laboratory-scale inverter prototype is built to validate the effectiveness of the proposed control method. Finally, conclusions are given in Sec. VII.

II. PRINCIPLE OF IMPEDANCE ENHANCEMENT

For the radial-line PV aggregated inverter system as depicted in Fig. 1, the output impedance of inverter with high magnitude and sufficient phase margin is more favorable to the system stability and dynamic performance. It provides a simple means for characterizing and comparing different inverter designs. However, increasing the inverter output impedance by the inverter’s own control is restricted by many factors, such as the digital delay and the output filter parameters. Moreover, with the number increase of paralleled inverters, the equivalent grid impedance viewed from single inverter is larger accordingly, which has detrimental effects on the system stability and power quality [8]. Therefore, it is necessary to focus on the study of the inverter output impedance. Our motivation in this paper is to strengthen the inverter output impedance and make all connected inverters passive over wide frequency range of interest.

In principle, a negative impedance, \(-Z_{o,k}\), connected in shunt at each inverter output of Fig. 1 will make the inverter output impedance infinite. Thus, a negative impedance, \(-\alpha \ast Z_{o,k}\), is proposed to connect in shunt with each inverter output impedance, \(Z_{o,k}\), as shown in Fig. 2(a). Considering that the shunted negative impedance might weaken the stability of the inverter, an active damping function, \(K_d \ast i_{k}\), is combined to ensure the passivity of the inverter as shown in Fig. 2(a).

Then, the equivalent inverter output impedance is increased to

\[
Z_{o,k}^* = \frac{-\alpha}{1-\alpha} Z_{o,k} + K_d \tag{1}
\]

where the impedance coefficient must meet \(\alpha \geq 1\) to avoid negative \(Z_{o,k}^*\). In particular, the inverter output impedance, \(Z_{o,k}^*\), increases towards infinity at the condition of \(\alpha = 1\). Then, the inverter is equivalent to an ideal current source and resists any grid disturbance.

Nevertheless, the shunted negative impedance, \(-\alpha \ast Z_{o,k}\), in Fig. 2(a) depends on the inverter output impedance and is difficult to obtain directly. In the paper, dual controlled voltage sources are proposed to replace the abovementioned negative impedance. Dual controlled voltage sources are only related to the node voltage, \(v_{o,k}/\alpha(k = 1, \ldots, n)\), and the injected current, \(i_k(k = 1, \ldots, n)\), both of which can be measured directly. As shown in Fig. 2(b), one of the added voltage sources is added in series at the inverter side, and the other is connected in series at the capacitor branch. After the above transformation, the shunted negative impedance, \(-\alpha \ast Z_{o,k}\), will be readily achieved through two controlled voltage sources. Detailed equivalent transformation from Fig. 2(a) to Fig. 2(b) can be found in Appendix.

III. SYSTEM DESCRIPTIONS WITH THE PROPOSED IMPEDANCE ENHANCEMENT MECHANISM

A. SYSTEM CONFIGURATION

The system configuration with the proposed impedance enhancement mechanism is shown in Fig. 3, where \(v_1\) and \(v_C\) represent the output voltage of the inverter and the filter capacitor voltage. \(i_1, i_1,\) and \(i_C\) respectively represent the inverter-side current, grid-side current, and filter capacitor current, and \(K_{pwm}\) represents the inverter gain. The LCL filter consists of an inverter-side inductor \(L_1\), a filter capacitor \(C_f\) and a grid-side inductor \(L_2\). For simplicity, only the main function of the inverter is illustrated in Fig. 3, which is composed of:

1) second-order generalized integrator phase-locked-loop (SOGI-PLL) for detecting the inverter output voltage, \(v_{o,1}\), and
2) current regulation by forcing the inverter output current, \(i_1\), to track the commanded current, \(i_{r,1}\).

In Fig. 3, the design rule of inverter current controller to ensure sufficient stability (i.e., phase margin > 45° and gain
margin > 10dB) under the stiff grid condition can be found in [42]. According to Fig. 2(b), the enhancement of the output impedance is achieved through two extra voltage-controlled voltage sources (VCVS) connected in series at the inverter side and the filter capacitor branch. The VCVS in series at the inverter side branch is merged into the inverter controller and does not require additional hardware circuit. As shown in Fig. 3, it is realized by a feedforward control strategy.

By contrast, another VCVS, $v_{pn}$, in series at the filter capacitor branch is realized by an additional low-voltage bidirectional voltage-source-converter (B-VSC) as shown in Fig. 3. The detailed circuit implementation is presented in Fig. 4(a), where two low-voltage MOSEFTs, S1 and S2, with very low $R_{DS(on)}$ are used as the switching devices, and the dc capacitor, $C_{dc}$, is used to maintain a very low dc voltage, $v_{dc}$. In practice, $v_{dc}$ is provided by the system auxiliary power supply or self-charging dc capacitor. Owing to low sustained voltage, such as $v_{dc} = 40V$, and small capacitor current through the B-VSC, the power wastage of the B-VSC is extremely low. Because the B-VSC only deals with harmonic impedance, the capacity of the B-VSC is small, and the cost is low. Thus, the B-VSC does not increase the cost of the several-kilowatt-level inverter. For safety reasons, the combination of Zener tube and resistor in shunt with the dc capacitor is used to avoid the unexpected high rectified voltage across the standby B-VSC.

### B. VOLTAGE REGULATION OF THE B-VSC

The output voltage, $v_{pn}$, of the B-VSC is composed of three major parts as follows.

1) The harmonic current of $i_1$, $i_{1,h} = K_d \cdot NF(i_1)$ is fed back to ensure the passivity of the inverter and simulate the positive resistor. It is responsible for the closed-loop control of $v_{pn}$. The gain of current feedback, $K_d$, will be designed in the following section.

2) Half of the dc capacitor voltage, $0.5v_{dc}$, is used to ensure the normal operation of the B-VSC. The dc offset injection does not participate the regulation of the inverter output impedance.

The transfer function of the notch filter (NF) can be expressed as:

$$G_{NF}(s) = \frac{s^2 + \omega_0^2}{s^2 + \omega_b \cdot s + \omega_0^2}$$

where $\omega_b$ represents the bandwidth of notch filter, and $\omega_0$ is the grid angular frequency.

Therefore, the total output voltage of the B-VSC is

$$v_{pn} = \text{NF}(v_o,1)/\alpha - K_d \cdot \text{NF}(i_1) + 0.5v_{dc}$$

where the feedforwarded dc voltage, $0.5v_{dc}$, does not affect the performance of the impedance reshaping.

The filter capacitor voltage, $v_c$, PCC voltage, $v_{pcc}$, the output voltage of the B-VSC, $v_{pn}$, and the average output voltage, avg($v_{pn}$), are given in Fig. 4(b). It can be seen that the output voltage of the B-VSC only contains the harmonic components of PCC voltage.

### IV. MODELING ANALYSIS

With the rapid performance advancements and cost reduction of digital signal processors (DSPs), digital implementations for controlling switching-mode power inverters have become...
A. INVERTER OUTPUT IMPEDANCE WITH THE TRADITIONAL CONTROL METHOD

Taking the digital delay and the PLL effects into account, the block diagram of the inverter with the traditional control method is presented in Fig. 5(a) [43], [44], where $G_{pll}(s)$ means the loop gain of the SOGI-PLL with the bandwidth of 30Hz, $I_m$ is thought as the constant of current reference, $G_C(s)$ represents the transfer function of the inverter-side current controller. $G_{d,1}(s)$ means the digital delay in the forward path of the inverter-side current controller. $G_{d,2}(s)$ represents the digital delay of PCC voltage feedforward and grid current feedback. Because the updates of \( \frac{v_{pcc}}{\omega} - K_d i_1 \) are prioritized by one sampling period compared to the updates of other algorithm results, $G_{d,2}(s)$ is approximately equivalent to the PWM delay brought by the zero-order hold [14]. $G_{d,1}(s)$ and $G_{d,2}(s)$ are approximated as

\[
G_{d,1}(s) \approx e^{-1.5sT_S} \tag{4a}
\]
\[
G_{d,2}(s) \approx e^{-0.5sT_S} \tag{4b}
\]

where $T_S$ represents the sampling cycle or execution cycle of the algorithm.

Based on Fig. 5(a), the inverter output impedance, $Z_o$, by using the traditional inverter-side current regulation with unit PCC voltage-feedforward control (VFFC) can be derived as (5), as shown at the bottom of the next page, where $\Delta_1$ is the characteristic transfer function of the loop gain expressed at the end of the next page.

By substituting the value tabulated in Table 1 into (5), the frequency response of the inverter output impedance and the grid impedance are plotted in Fig. 6. It is observed that the phase of the inverter output impedance is close to $\pm 90^\circ$ over a wide range of frequencies, and the passivity of the inverter output impedance is too weak to ensure the system stability in different grid conditions. As shown in the figure, the phase difference at one intersection frequency between the inverter output impedance and the grid impedance tends to $180^\circ$ with the increase of grid impedance, which will arouse instability easily.

B. INVERTER OUTPUT IMPEDANCE WITH THE PROPOSED CONTROL METHOD

By adopting the proposed impedance enhancement mechanism introduced in Sec. III, the control block diagram of the inverter can be drawn in Fig. 5(b), where the notch filter is used to eliminate the fundamental frequency component of \( \frac{v_{pcc}}{\omega} - K_d i_1 \) so that the B-VSC only tracks the harmonic component and sustain a very low power capacity. It should be noted that both the effects of notch filter and the dc offset, $0.5v_{dc}$, in (3) are neglected for simplifying the following analysis.

According to Fig. 5(b), the enhanced inverter output impedance, $Z_o^*$, is derived as (6), as shown at the bottom of the next page, where $M(s) = (sC_f G_C(s) G_{d,1}(s) + s^2L_1 C_f)$, and $\Delta_2$ is the characteristic transfer function of the loop gain expressed at the end of this page.

To ensure sufficient passivity of the inverter output impedance with the proposed control method, the value of $K_d$ and $\alpha$ in Fig. 5(b) must be designed properly. The design of these parameters is based on the following criterion:

1) DESIGN OF $K_d$

Based on Fig. 20(d), it is known that the characteristic resonant frequency of filter varies with $K_d$. For instance,
if \( K_d = 0 \Omega \), the maximum characteristic resonant frequency is

\[
\omega_{r_{\text{up}}} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{7}
\]

Similarly, the minimum characteristic resonant frequency is obtained when \( K_d = \infty \Omega \)

\[
\omega_{r_{\text{down}}} = \sqrt{\frac{1}{L_1 C_f}} \tag{8}
\]

Second, the impedance expression of \( L_1 \) and branch \( L_2 - K_d \) is calculated as

\[
Z_{L(LCL)} = \frac{s L_1 (s L_2 + K_d)}{s L_1 L_2 + L_1 + K_d} \tag{9}
\]

of which impedance feature can be further plotted as Fig. 7.\[
\Delta_1 = s^3 L_1 L_2 C_f + s^2 L_2 C_f G_C (s) G_{d,1} (s) + s (L_1 + L_2) + G_C (s) G_{d,1} (s) \tag{10a}
\]
\[
\Delta_2 = s^2 C_f (s L_1 L_2 + L_2 G_C (s) G_{d,1} (s) + L_1 K_d G_{d,2} (s) G_{NF} (s)) + s (L_1 + L_2) + G_C (s) G_{d,1} (s) G_{NF} (s) + 1 + K_d G_{d,2} (s) \tag{10b}
\]

To damp the LCL filter resonance, the changeable resonant frequencies between (7) and (8) should locate at the resistive region in Fig. 7. Accordingly, based on (9), The described circumstance is shown as

\[
\frac{K_d}{L_1 + L_2} \leq \omega_r \leq \frac{K_d}{L_2} \tag{11}
\]

Then combining (7) and (8), the constraint condition based on the virtual resistance concept can be derived as

\[
\begin{align*}
\frac{K_d}{L_1 + L_2} & \leq \omega_{r_{\text{down}}} \\
\frac{K_d}{L_2} & \geq \omega_{r_{\text{up}}}
\end{align*} \tag{12}
\]

Based on (12) and Table 1, the effective range of \( K_d \) is calculated as \( 23.35 \leq K_d \leq 40.45 \).

2) DESIGN OF \( \alpha \)

As described in Sec. II, \( \alpha \) is used to balance the impedance enhancement and the passivity of the inverter output impedance. For example, if \( \alpha = 1 \), the inverter output impedance is maximized. However, the positive feedback of the PCC voltage as shown in Fig. 5(b) inevitably introduces negative effects on the system stability [34], [45]. In this respect, \( \alpha \) should be increased to ensure sufficient passivity of the inverter output impedance. Define that the phase margin of the inverter output impedance in the frequency range of interest (i.e., from 0.1kHz to 10kHz) is over 40°. Then, according to the phase surface drawn in Fig. 8, it is easy to find the effective range of \( \alpha \) is \( \alpha \geq 1.18 \).

To sum up, \( K_d \) and \( \alpha \) can be chosen as \( K_d = 40 \) and \( \alpha = 1.2 \). Then, the frequency response of the inverter output impedance with the proposed impedance enhancing control mechanism are plotted in Fig. 9, and compared with different grid impedance. It indicates that the phase of the inverter output impedance is maintained within \([−50°, 0°]\) over a wide frequency range, and sufficient phase margin is achieved. Thus, the inverter maintains sufficient stability even if the grid impedance changes widely.

V. SIMULATION RESULTS

In this section, the proposed strategy for enhancing the inverter output impedance is tested by means of numerical
FIGURE 8. Phase surface of the output impedance against the values of $\alpha$ and $f$ ($K_d = 40$).

FIGURE 9. Frequency response of the inverter output and grid impedance with the proposed control scheme ($\alpha = 1.2$ and $K_d = 40$).

simulation using the simulation tool. In simulation, it is defined that 16 inverter modules are paralleled through the distributed feeder impedance. Comparative performance of the radial-line inverter system with the traditional control method and the proposed control method are studied. System parameters of the case study are tabulated in Table 1, where

the inverters are connected to each other through the 0.1km equivalent cable models [18], [26].

By using the traditional inverter-current-feedback control based on PI with unit PCC voltage feedforward, the system is stable in the stiff grid as shown in Fig. 10(a), where $I(S1.L2)$, $I(S5.L2)$, $I(S9.L2)$, and $I(S13.L2)$ are the inverter output current at bus #1, #5, #9, and #13, respectively. However, with the increase of grid impedance, the system stability becomes worse until instability happens, which matches with Fig. 6 in Sec. IV. That is because the intersection phase difference between the inverter output and equivalent grid impedance is beyond $180^\circ$ as analyzed Sec. IV-A. By using the proposed control method, owing to the passivity of the inverter output impedance over a wide frequency range as analyzed in Sec. IV-B, the system maintains sufficient stability even under wide change of the grid impedance as presented in Fig. 10(b). It should be noted that the grid impedance $L_g$ is amplified 16 times in terms of single inverter if all inverters with control are identical.

To evaluate the impacts of the inverter outage on the capability of the proposed method, the inverters at different buses are cut off in order as presented in Fig. 11, where $i_g$ represents the grid current. As the inverters shut down one by one, $i_g$ is decreasing gradually and stably. It indicates that the outage of the inverters has no impacts on the performance of inverters with the proposed method. That is because the proposed method ensures sufficient passivity of the inverter output impedance over a wide range of frequencies, and the system stability is not constraint by the change of equivalent grid impedance.
VI. EXPERIMENTAL VALIDATION

In order to verify the effectiveness of the proposed impedance enhancing control mechanism experimentally, a 3-paralleled laboratory inverter prototype has been built and evaluated. The inverters are supplied by three external DC power supplies, and the control is implemented by the digital controllers, Texas Instruments TMS320F28379D. The operation frequency of the inverter and the B-VSC is 20kHz and 40kHz, respectively.

The system structure with variable grid impedance is presented in Fig. 12, where the inverter system feeds into a power grid through an isolator for the safety reason. Fig. 13 shows the experimental test platform photo. The B-VSC is activated before the inverter is enabled. Thereafter, the inverter can work stably.

A. COMPARATIVE RESULTS WITH TRADITIONAL METHOD

The performances of a 3-parallel inverter system under different control schemes are compared in the following. The steady-state waveforms of traditional well-designed inverters under different grid impedance are depicted in Fig. 14. It reveals that the inverter with unit PCC voltage feedforward is resistive to grid disturbances. However, on account of significant phase difference at the intersection points between \(Z_o\) and \(Z_g\) as plotted in Fig. 6, the system stability becomes weaker and causes PCC voltage oscillation (THD = 8.6%) in the weak grid (i.e., \(L_g = 15\text{mH}\)). If the
parallel inverter number is large, such serious distortion of PCC voltage caused by the inverters is propagated through feeder impedance and could arouse the system harmonic instability as simulated in Sec. V.

Such problem is addressed well by adding the proposed impedance enhancer into the inverter. Fig. 15 shows the corresponding results under different grid conditions. As detected by HIOKI 3196, the total harmonic distortion (THD) of the inverter side current and PCC voltage at the condition of \( L_g = 15 \text{mH} \) in Fig. 15(b) is only 1.1% (VSI #1) and 2.2%, respectively. Even with highly distorted PCC voltage (THD = 12.5%) caused by the shunted nonlinear rectifying load at the PCC, the current THD is still sustained at 2.3% (VSI #1) as shown in Fig. 16.

**FIGURE 15.** Steady-state waveforms of the proposed control method. (a) \( L_g = 0 \text{mH} \). (b) \( L_g = 15 \text{mH} \).

**FIGURE 16.** Steady-state waveforms of the proposed control method with the shunted nonlinear rectifying load at the PCC (\( L_g = 15 \text{mH} \)).

**FIGURE 17.** System startup (\( L_g = 15 \text{mH} \)).

**FIGURE 18.** Key waveforms when the inverter outage occurs (\( L_g = 15 \text{mH} \)).

**B. DYNAMIC BEHAVIOR**

During the system startup as shown in Fig. 17, the 3-paralleled inverters get ready in order and generate the high-quality power into the grid, of which the integrated impedance enhancer gets involved soon. Fig. 18 indicates that the outage of the inverters does not harm the system stability. That is because all inverters with the proposed control method have been designed passively, and the change of equivalent grid impedance has minor impacts on the impedance enhancing capability.

**C. DISCUSSIONS ON THE B-VSC**

The steady-state waveforms of the B-VSC under the weak grid condition are shown in Fig. 19, where \( i_{dc} \) is the bus current of the B-VSC with an average value of only 5.14mA, \( i_c \) is the output current of the B-VSC or the filter capacitor current with a root-mean-square (RMS) value of 0.5A, and \( i_1 \) is the grid current of inverter #2. In order to facilitate the design of the B-VSC, the following will briefly discuss its DC power supply mode, maximum capacity, power loss, and applicable occasions.

1) The DC power supply voltage of the B-VSC should be higher than the amplitude of grid harmonic voltage. For
example, the DC power supply voltage of the B-VSC is chosen as 40V in our experimental prototype. Owing to extra low power capacity, the dc voltage can be supplied by adding a winding to the auxiliary power supply transformer.

2) The maximum power capacity required by the B-VSC can be roughly estimated by the product of the DC voltage and the RMS value of the filter capacitor current.

3) The power loss of the B-VSC mainly comprises of the conduction loss of switching devices and DC capacitors, which is determined by the filter capacitor current. Since the filter capacitor current is small, the loss of the B-VSC will not sacrifice the inverter efficiency.

4) Since the B-VSC is in series with the filter capacitor and only deals with harmonic power, the B-VSC is also suitable for high-voltage and high-power grid-connected inverters.

VII. CONCLUSION
An inverter output impedance enhancing control mechanism has been proposed and derived in the paper. Its control functions are described in detail, and control parameters are designed based on the passivity-based stability criterion. As studied, the proposed architecture guarantees sufficient passivity of each inverter in the radial-line DPGS and strong resistance to grid disturbances even with irregular load at the grid side and under ultra-wide variable grid conditions. Moreover, the control performance of the proposed impedance enhancer is not weakened by the outage of parallel inverters. The effectiveness of the proposed method has been verified on a 16-parallel radial-line inverter simulation platform and a 3-parallel laboratory-scale inverter testbed.

APPENDIX
The shunted negative impedance, \(-\alpha \ast Z_{o,k}\), in Fig. 2(a), can be converted to the voltage-controlled current source, \(\frac{V_{o,k}}{\alpha Z_{o,k}}\), controlled by the node voltage, \(V_{o,k}\), as presented in Fig. 20(a). Then, the combined current source at each node becomes \((i_{r,k} + \frac{V_{o,k}}{\alpha Z_{o,k}})\). According to equivalent transformation from Norton’s circuit to Thevenin’s circuit, Fig. 20(a) is converted to Fig. 20(b), in which the function of the series voltage sources, \(\frac{V_{o,k}}{\alpha}\), is equivalent to the shunted negative impedance in Fig. 2(a). Then, by an operation similar to the equivalent transformation described above, the voltage sources, \(i_{r,k} \ast Z_{o,k}\), in series with \(Z_{o,k}\) are changed back to the current sources, \(i_{r,k}\), in shunt with \(Z_{o,k}\) as presented in Fig. 20(c). Finally, by transforming the impedance-based modeling circuit into the original one-line diagram of the inverter system with LCL filters, Fig. 20(d) is obtained.

Taking the inverter #1 as an example, based on KVL, the relationship among the PCC voltage, \(V_{o,1}\), the filter voltage, \(V_{L,1}, V_{L,2}\), and \(V_C\), and the series voltage at the inverter output,
\[
\left(\frac{v_{o,1}}{\alpha} - K_{d1}i_1\right), \text{ is derived as}
\]
\[v_{o,1} + v_{L,2} = \left(\frac{v_{o,1}}{\alpha} - K_{d1}i_1\right) = vC = vL - vL_1, \quad \text{(A.1)}
\]

Eq. (A1) can be rewritten into
\[v_{o,1} + v_{L,2} = vC + \left(\frac{v_{o,1}}{\alpha} - K_{d1}i_1\right)
= vL - vL_1 + \left(\frac{v_{o,1}}{\alpha} - K_{d1}i_1\right), \quad \text{(A.2)}
\]

where the voltage source, \(\left(\frac{v_{o,1}}{\alpha} - K_{d1}i_1\right)\), in series at the inverter output as written in (A1) can be converted into two equivalent voltage sources as shown in (A2), in which one is in the filter capacitor branch, and the other is in series with the inverter-side inductor. Such voltage separation can be expanded to all remained nodes. Finally, Fig. 2(a) is transformed to Fig. 2(b).

REFERENCES


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