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A Novel Topology Derivation Method Revealed from Classical Cuk, Sepic, and Zeta Converters

Liping Mo, *Member, IEEE*, Yibo Wang, *Member, IEEE*, C. Q. Jiang, *Senior Member, IEEE*, Xiaosheng Wang, Ben Zhang

***Abstract*—The classical Cuk, Sepic, and Zeta converters have found wide applications in various fields. However, there has been limited research exploring their relationships. This letter aims to uncover their relationships by focusing on their capacitor-less circuits (CLCs). Initially, it is observed that these three converters exhibit highly similar performance characteristics, such as equal voltage gains and average component currents. Subsequently, this letter establishes that their equivalent CLCs are the reason behind these similarities, presenting a new perspective on understanding dc-dc converters with capacitors. Furthermore, based on the above findings, a novel topology derivation method is proposed by connecting capacitors to a CLC. Compared with the traditional methods, the proposed method can derive families of converters with comparable performance. Moreover, the proposed method is particularly suitable to leverage existing converter designs and modify them to meet specific requirements. The proposed method successfully derives several groups of converters from different CLCs. For a group of converters derived from an equivalent CLC, their effectiveness and their performance relationship are verified experimentally.**

***Index Terms*—dc-dc converters, topology derivation, capacitor-less-circuits**

I. INTRODUCTION

DC-DC converters have been widely utilized in motor drives, renewable energy systems, and electric vehicles [1], [2]. More converters are required to satisfy the diverse requirements in practical applications.

Studying inherent relationships, especially the similarity among existing converters, is an intuitive and basic approach to find new converters. One of the most typical examples is developing topology derivation methods by exploring the relationships among classical Buck, Boost, and BuckBoost converters [3]. Paper in [3] finds that after these three converters' input and output ports are removed, their corresponding remaining circuits, namely, three-terminal cells, are equivalent. Hence, these three converters can be seen as two voltage ports connected at different positions of an equivalent three-terminal cell. Inspired by [3], more three-terminal cells with different circuit configurations are designed to derive new converters [4], [5], [6]. For example, in [4], the concept of a three-terminal cell is extended to develop a systematic method to generate families of dc-dc converters by flipping the three-terminal cells of existing converters. Besides, in [6], a three-terminal cell with a coupled inductor is designed to derive families of dc-dc converters with high voltage gains. It is noted that the relationships among other kinds of converters can also be summarized to develop topology derivation methods [7], [8], [9]. In [7], after the relationship among existing single-inductor multi-port (SI-MP) converters is explored, a unified cell made up of an inductor and several switches is proposed to derive SI-MP converters. Similarly, [8] and [9] summarize the derivation principle from several converters with bidirectional ports and propose an H-bridge cell and storage-switch-diode cell to derive new topologies with bidirectional ports. Hence, investigating the relationships among existing converter topologies not only improves the understanding of those converters but also facilitates the derivation of new topologies.

Classical Cuk, Speic, and Zeta are three well-recognized converters for their step-up and step-down voltage conversion capabilities. Some research has found that they can be changed each other by rearranging components [10]. However, little research points out that they have highly similar performance characteristics including equal voltage gains and average component currents. This letter will try to investigate their inherent relationships and then develop a new topology derivation method. The main contributions of this letter are as follows:

- **Contribution 1**: Reveal relationships among Cuk, Sepic, and Zeta converters from their capacitor-less circuits (CLCs).
- **Contribution 2**: Propose a novel topology derivation method based on CLC to find families of converters with comparable performance characteristics.

The remainder of the letter is organized as follows. In Section II, the relationships among Cuk, Sepic, and Zeta converters are analyzed. In Section III, a topology derivation method based on CLC is proposed. The proposed method is utilized to derive families of converters in Section IV. Seven converters derived from an equivalent CLC are verified experimentally in Section V. Finally, the conclusion is given in Section VI.

II. RELATIONSHIPS AMONG CUK, SEPIC, AND ZETA CONVERTERS

This section reveals the relationships among Cuk, Sepic, and Zeta converters, including their performance and topology relationships.

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Performance relationship (PR): Cuk, Sepic, and Zeta converters demonstrate remarkably similar performance characteristics [10]. They share the same voltage gains, as well as comparable voltage stresses on switches and diodes, inductor voltage in each switching mode, and average currents through all components. The main difference lies in the capacitor voltages.

Topology relationship (TR): Due to the performance difference arising from capacitor, an intuitive idea is to remove the capacitor from the converters, resulting in their CLCs (CLC_{Cuk}, CLC_{Sepic}, and CLC_{Zeta}), as shown in Fig. 1. It is observed that CLCs of these converters are equivalent since they can be transformed into each other by swapping the series-connected components or reversing polarity of components. For example, CLC_{Sepic} can be transferred into CLC_{Zeta} by swapping its L_1 and S_1 and then swapping its L_2 and D_1. More precisely, as illustrated in Fig. 1, the three CLCs shared the same loops (lp_1~lp_3), demonstrating their equivalence [11]. Therefore, Cuk, Sepic, and Zeta can be viewed as three converters with capacitors connected in different positions of an equivalent CLC.

Relation between PR and TR: Comparable performance characteristics among Cuk, Sepic, and Zeta converters can be attributed to their equivalent CLCs. Since capacitors inherently have zero average currents to maintain ampere-second balance, changing their positions does not affect the average currents of converters. Therefore, all these converters exhibit equal average currents across their components. Consequently, since their average output currents are equal, the output voltage of these converters are also the same. Additionally, as the voltage across a capacitor is determined passively by the surrounding components, which means changing the capacitor positions in converters will not change the voltages of any components except capacitors. Hence, these converters exhibit equal voltages across all components except capacitors.

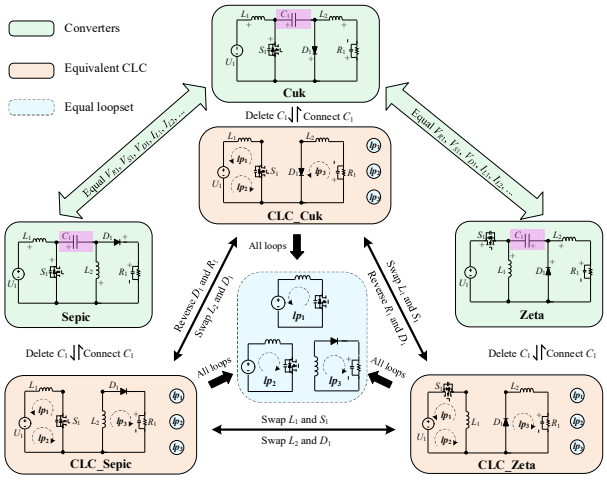


Fig. 1. Cuk, Sepic, Zeta converters, their CLCs, and loops of CLCs.

III. Topology Derivation Method Based on CLC

Inspired by the similarities among Cuk, Sepic, and Zeta converters, Fig. 2 proposes a method to derive new topologies. This method begins with a CLC and several capacitors. By connecting capacitors to the nodes $\{a_1, a_2, \ldots, a_n\}$ in the CLC and applying effective converter constraints [12], families of converters with similar performance can be easily derived.

Design of CLC: CLC is composed of any components except capacitors. CLC should be designed to satisfy the following two basic principles so that it can be used to derive effective topologies. (i) Any components in CLC cannot be suspended since the average current of the suspended component will be zero. (ii) There should be no less than two loops in CLC.

Features of derived topologies: According to the analysis in Section II, converters derived from an equivalent CLC have similar performance characteristics including the same voltage gains, as well as comparable voltage stresses on switches and diodes, inductor voltages across switching modes, and average currents through all components. While capacitor voltages and the instantaneous component currents may be different.

With a designed CLC, a family of converters with similar performance characteristics can be found. More importantly, CLCs can also be extracted from existing converters. With these extracted CLCs, one can easily modify aspects such as capacitor voltages, port grounding configurations, and the continuity of port currents in the existing converters.

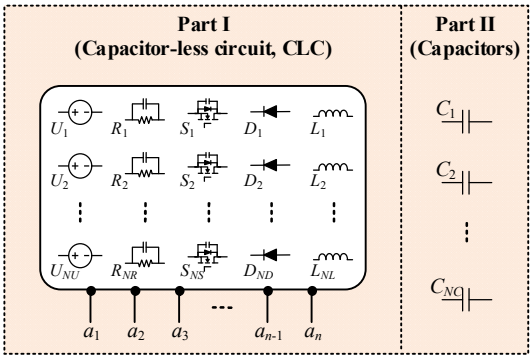


Fig. 2. Topology derivation method based on CLC.

IV. Implementation of CLC-based Method

To verify the method's feasibility, we design 4 CLCs with 1 switch, 1 diode, 2 inductors, 1 input, and 1 output in Table I. After a capacitor is connected to the potential positions of CLC (a_1~a_5), two topologies are derived from each CLC, as shown in

Table I. Derived topologies from four designed CLCs.

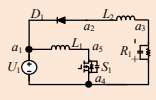
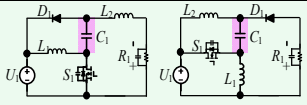
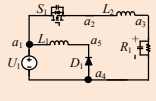
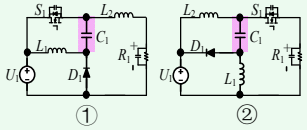
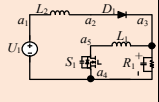
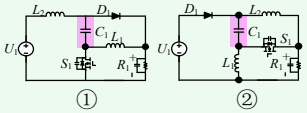
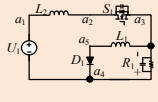
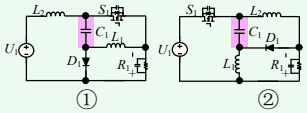
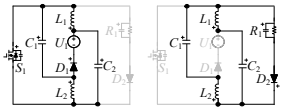
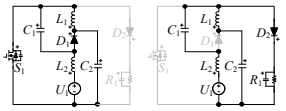
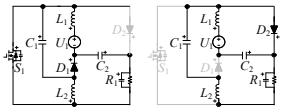
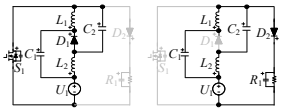
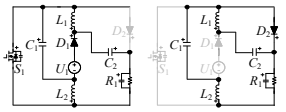
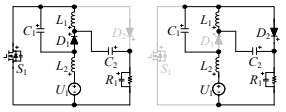
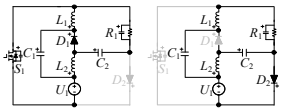
No.	V_{R1}, V_{S1}, V_{D1}	CLC	Derive topologies
I	$V_{R1}=\frac{2d-1}{1-d}V_{U1}$ $V_{S1}=V_{U1}$ $V_{D1}=\frac{d}{1-d}V_{U1}$		
II	$V_{R1}=\frac{2d-1}{d}V_{U1}$ $V_{S1}=\frac{1-d}{d}V_{U1}$ $V_{D1}=V_{U1}$		
III	$V_{R1}=\frac{d-1}{2d-1}V_{U1}$ $V_{S1}=\frac{d-1}{2d-1}V_{U1}$ $V_{D1}=\frac{d}{2d-1}V_{U1}$		
IV	$V_{R1}=\frac{d}{2d-1}V_{U1}$ $V_{S1}=\frac{3d-1}{2d-1}V_{U1}$ $V_{D1}=\frac{d}{2d-1}V_{U1}$		

Table I. Taking the No.1 CLC in Table I as an example, the topology derivation processes are as follows. First, the capacitor C_1 is connected to a_1~a_5 arbitrarily to select an effective topology, as the topology ① of No.1 CLC is shown in Table I. Then, a CLC that is equivalent to the No.1 CLC is obtained by swapping the series-connected components, and by connecting capacitor C_1 to this CLC, topology ② of No.1 CLC in Table I is derived. It is noted that labels of nodes (a_1~a_5) in CLC represent the relative positions of the nodes, rather than the physical connecting point between components. Hence, although the physical connecting points are changed when the series-connected components are moved, the relative positions of the nodes can be considered unchanged, and labels of nodes can be maintained consistently to complete deriving topologies. All eight topologies in Table I are all newly derived in this letter, and their output voltage V_{R1}, voltage stresses of switch and diode (V_{S1} and V_{D1}) are also illustrated in Table I. It can be found that topologies from the same CLC always have similar performance characteristics, which agrees with the previous analysis.

CLC can also be extracted from an existing converter. For example, a CLC is extracted from the converter in [13]. By changing the connected positions of two capacitors, six new topologies are derived in Table II. All seven converters in Table II are analyzed and their steady-state performance characteristics and port configurations are compared in Table III. With Table III, it can be found that these seven converters have the same V_{R1}, V_{S1}, V_{D1}~V_{D2}, I_{U1}, I_{R1}, and I_{L1}~I_{L2}, which validates that converters derived from an equivalent CLC should have similar performance. These seven converters exhibit the following different performance. For example, their capacitor voltages V_{C1}~V_{C2} are different, and topologies ④⑥ present the lowest capacitor voltages among the seven converters, which means topologies ④⑥ can use capacitors with smaller sizes and lower

Table III Performance comparison of seven converters derived in Table II. (d is the duty cycle of switch S_1, $0<d<0.5$)

No.	Switching modes	Output voltage (V_{R1}) Switch voltage stress (V_{S1}) Diode voltages stresses (V_{D1}~V_{D2})	Inductor currents (I_{L1}~I_{L2}) Average input current (I_{U1}) Average output current (I_{R1})	Capacitor voltages (V_{C1}~V_{C2})	Instantaneous input currents ($i_{U1\text{-}SM1}$~ $i_{U1\text{-}SM2}$)	Instantaneous output currents ($i_{R1\text{-}SM1}$~ $i_{R1\text{-}SM2}$)	Ports with continuous current	Floating/ common ground
①	 (SM1) (SM2)	$\frac{V_{R1}}{V_{U1}}=\frac{1}{1-2d}$ $\frac{V_{S1}}{V_{U1}}=\frac{1}{1-2d}$ $\frac{V_{D1}}{V_{U1}}=\frac{1}{1-2d}$ $\frac{V_{D2}}{V_{U1}}=\frac{1}{1-2d}$	$\frac{I_{L1}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$ $\frac{I_{L2}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$ $\frac{I_{U1}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$ $\frac{I_{R1}}{V_{U1}}=\frac{1}{R_1(1-2d)}$	$\frac{V_{C1}}{V_{U1}}=\frac{1-d}{1-2d}$ $\frac{V_{C2}}{V_{U1}}=\frac{1-d}{1-2d}$	$\frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{1}{R_1d(1-2d)^2}$ $\frac{i_{U1\text{-}SM2}}{V_{U1}}=0$	$\frac{i_{R1\text{-}SM1}}{V_{U1}}=0$ $\frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)(1-d}$	None	Floating
②	 (SM1) (SM2)			$\frac{V_{C1}}{V_{U1}}=\frac{d}{1-2d}$ $\frac{V_{C2}}{V_{U1}}=\frac{1-d}{1-2d}$	$\frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$ $\frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$	$\frac{i_{R1\text{-}SM1}}{V_{U1}}=0$ $\frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)(1-d}$	Input port U_1	Common ground
③	 (SM1) (SM2)			$\frac{V_{C1}}{V_{U1}}=\frac{1-d}{1-2d}$ $\frac{V_{C2}}{V_{U1}}=\frac{1-d}{1-2d}$	$\frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$ $\frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$	$\frac{i_{R1\text{-}SM1}}{V_{U1}}=\frac{-1}{R_1(1-2d)^2}$ $\frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$	Input port U_1	Floating
④	 (SM1) (SM2)			$\frac{V_{C1}}{V_{U1}}=\frac{d}{1-2d}$ $\frac{V_{C2}}{V_{U1}}=\frac{d}{1-2d}$	$\frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{2}{R_1(1-2d)^2}$ $\frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)(1-}$	$\frac{i_{R1\text{-}SM1}}{V_{U1}}=0$ $\frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)(1-d}$	None	Common ground
⑤	 (SM1) (SM2)			$\frac{V_{C1}}{V_{U1}}=\frac{1-d}{1-2d}$ $\frac{V_{C2}}{V_{U1}}=\frac{d}{1-2d}$	$\frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{1}{R_1d(1-2d)^2}$ $\frac{i_{U1\text{-}SM2}}{V_{U1}}=0$	$\frac{i_{R1\text{-}SM1}}{V_{U1}}=\frac{-1}{R_1(1-2d)^2}$ $\frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$	None	Floating
⑥	 (SM1) (SM2)			$\frac{V_{C1}}{V_{U1}}=\frac{d}{1-2d}$ $\frac{V_{C2}}{V_{U1}}=\frac{d}{1-2d}$	$\frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$ $\frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$	$\frac{i_{R1\text{-}SM1}}{V_{U1}}=\frac{-1}{R_1(1-2d)^2}$ $\frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$	Input port U_1	Common ground
⑦	 (SM1) (SM2)			$\frac{V_{C1}}{V_{U1}}=\frac{d}{1-2d}$ $\frac{V_{C2}}{V_{U1}}=\frac{1-d}{1-2d}$	$\frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{2}{R_1(1-2d)^2}$ $\frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)(1-}$	$\frac{i_{R1\text{-}SM1}}{V_{U1}}=\frac{-1}{R_1(1-2d)^2}$ $\frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1}{R_1(1-2d)^2}$	None	Floating

costs. Besides, port configurations among these seven converters are also different. For instance, topologies ② ④ ⑥ have configuration of common ground ports, while ports in topologies ①③⑤⑦ are floating. Currents of input ports are continuous in topologies ②③⑥ while discontinuous in topologies ①④⑤⑦. Compared with the existing topology ①, the newly derived topologies ② ⑥ exhibit several improvements, like lower capacitor voltage and common ground ports, providing more choices in practical applications. Further, we extract another CLC from the converter in [14], and another 6 converters, including one in [15], two in [16], and three new converters, are derived in Table IV. Therefore, the proposed method allows more comprehensive deriving of converters with similar performance characteristics. These converters are analyzed and compared in Table V. Similar as the derived results in Table II, all seven converters in Table IV exhibit similar performance like equal output voltage and switch voltage stress while their capacitor voltages and port configurations may be different.

In summary, compared with the traditional topology derivation methods in [3-9], the proposed method is easy to operate and especially suitable for finding new topologies from existing converters by exacting their CLCs.

Table IV. Derived topologies from the CLC extracted from the converter in [14].

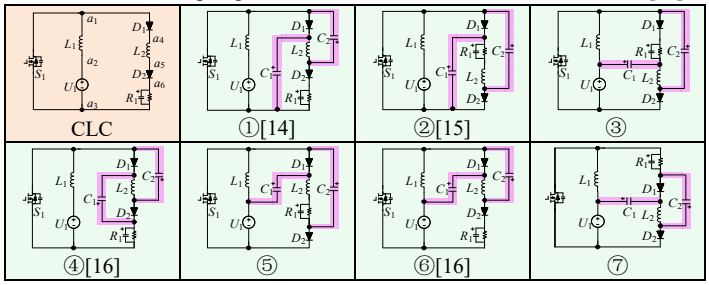
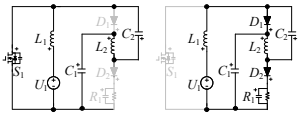
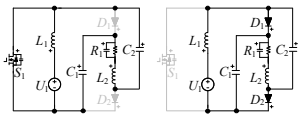
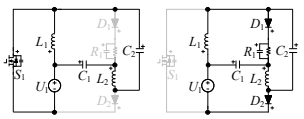
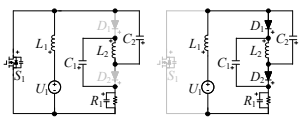
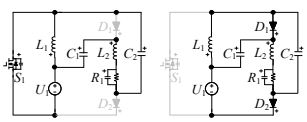
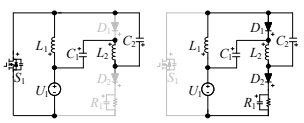
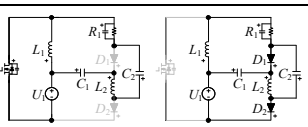


Table V Performance comparison of seven converters derived in Table IV. (d is the duty cycle of switch S_1, $0<d<1$)

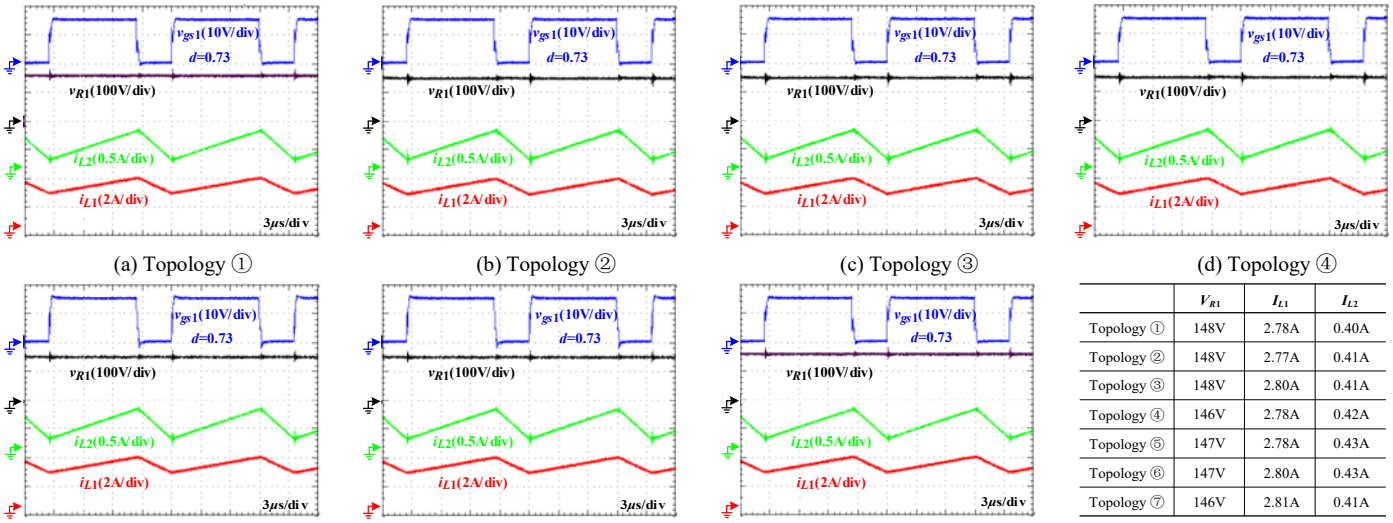
No.	Switching modes	Output voltage (V_{R1}) Switch voltage stress (V_{S1}) Diode voltage stresses (V_{D1}~V_{D2})	Inductor currents (I_{L1}~I_{L2}) Average input current (I_{U1}) Average output current (I_{R1})	Capacitor voltages (V_{C1}~V_{C2})	Instantaneous input currents ($i_{U1\text{-}SM1}$~ $i_{U1\text{-}SM2}$)	Instantaneous output currents ($i_{R1\text{-}SM1}$~ $i_{R1\text{-}SM2}$)	Ports with continuous current	Floating/ common ground
①	 (SM1) (SM2)	$\begin{cases} \frac{V_{R1}}{V_{U1}}=\frac{d+1}{1-d} \\ \frac{V_{S1}}{V_{U1}}=\frac{1}{1-d} \\ \frac{V_{D1}}{V_{U1}}=\frac{1}{1-d} \\ \frac{V_{D2}}{V_{U1}}=\frac{1}{1-d} \end{cases}$	$\begin{cases} \frac{I_{L1}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \\ \frac{I_{L2}}{V_{U1}}=\frac{(1+d)}{R_1(1-d)} \\ \frac{I_{U1}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \\ \frac{I_{R1}}{V_{U1}}=\frac{(1+d)}{R_1(1-d)} \end{cases}$	$\begin{cases} \frac{V_{C1}}{V_{U1}}=\frac{1}{1-d} \\ \frac{V_{C2}}{V_{U1}}=\frac{d}{1-d} \end{cases}$	$\begin{cases} \frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \\ \frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \end{cases}$	$\begin{cases} \frac{i_{R1\text{-}SM1}}{V_{U1}}=0 \\ \frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1+d}{R_1(1-d)^2} \end{cases}$	Input port U_1	Common ground
②	 (SM1) (SM2)			$\begin{cases} \frac{V_{C1}}{V_{U1}}=\frac{1}{1-d} \\ \frac{V_{C2}}{V_{U1}}=\frac{1}{1-d} \end{cases}$	$\begin{cases} \frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \\ \frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \end{cases}$	$\begin{cases} \frac{i_{R1\text{-}SM1}}{V_{U1}}=\frac{1+d}{R_1(1-d)} \\ \frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1+d}{R_1(1-d)} \end{cases}$	Input port U_1 & Output port R_1	Floating
③	 (SM1) (SM2)			$\begin{cases} \frac{V_{C1}}{V_{U1}}=\frac{1}{1-d} \\ \frac{V_{C2}}{V_{U1}}=\frac{1}{1-d} \end{cases}$	$\begin{cases} \frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{2(1+d)}{R_1(1-d)^2} \\ \frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{(1+d)}{R_1(1-d)^2} \end{cases}$	$\begin{cases} \frac{i_{R1\text{-}SM1}}{V_{U1}}=0 \\ \frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1+d}{R_1(1-d)^2} \end{cases}$	None	Floating
④	 (SM1) (SM2)			$\begin{cases} \frac{V_{C1}}{V_{U1}}=\frac{d}{1-d} \\ \frac{V_{C2}}{V_{U1}}=\frac{d}{1-d} \end{cases}$	$\begin{cases} \frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \\ \frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \end{cases}$	$\begin{cases} \frac{i_{R1\text{-}SM1}}{V_{U1}}=\frac{-(1+d)}{R_1(1-d)} \\ \frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \end{cases}$	Input port U_1	Common ground
⑤	 (SM1) (SM2)			$\begin{cases} \frac{V_{C1}}{V_{U1}}=\frac{d}{1-d} \\ \frac{V_{C2}}{V_{U1}}=\frac{1}{1-d} \end{cases}$	$\begin{cases} \frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{2(1+d)}{R_1(1-d)^2} \\ \frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{(1+d)}{R_1(1-d)^2} \end{cases}$	$\begin{cases} \frac{i_{R1\text{-}SM1}}{V_{U1}}=\frac{1+d}{R_1(1-d)} \\ \frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1+d}{R_1(1-d)} \end{cases}$	Output port R_1	Floating
⑥	 (SM1) (SM2)			$\begin{cases} \frac{V_{C1}}{V_{U1}}=\frac{d}{1-d} \\ \frac{V_{C2}}{V_{U1}}=\frac{d}{1-d} \end{cases}$	$\begin{cases} \frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{2(1+d)}{R_1(1-d)^2} \\ \frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{(1+d)}{R_1(1-d)^2} \end{cases}$	$\begin{cases} \frac{i_{R1\text{-}SM1}}{V_{U1}}=0 \\ \frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{1+d}{R_1(1-d)^2} \end{cases}$	None	Common ground
⑦	 (SM1) (SM2)			$\begin{cases} \frac{V_{C1}}{V_{U1}}=\frac{1}{1-d} \\ \frac{V_{C2}}{V_{U1}}=\frac{d}{1-d} \end{cases}$	$\begin{cases} \frac{i_{U1\text{-}SM1}}{V_{U1}}=\frac{2(1+d)}{R_1(1-d)^2} \\ \frac{i_{U1\text{-}SM2}}{V_{U1}}=\frac{(1+d)}{R_1(1-d)^2} \end{cases}$	$\begin{cases} \frac{i_{R1\text{-}SM1}}{V_{U1}}=\frac{-(1+d)}{R_1(1-d)} \\ \frac{i_{R1\text{-}SM2}}{V_{U1}}=\frac{(1+d)^2}{R_1(1-d)^2} \end{cases}$	None	Floating

V. Experimental Verification

Seven prototype circuits of topologies ①~⑦ in Table IV are developed to verify their effectiveness and their performance relationships experimentally. The system and hardware parameters of these prototypes are set as follows: input voltage V_{U1}=24V, output voltage V_{R1}=150V, output resistance R_1=360Ω, inductance L_1=150μH and L_2= 300μH, capacitance C_1=C_2=100μF, Mosfet IPP530N15N3 is chosen for switch S_1, two MUR1520G are chosen for diodes D_1~D_2, and switching frequency is set as 100kHz.

Defined duty cycle of switch S_1 as d, topologies ①~⑦ in Table IV should have equal output voltage $V_{R1} = V_{U1}(1+d)/(1-d)$, and the theoretical value of d should be 0.72 to satisfy the required voltage conversion. As shown in Fig. 3(a)~(g), when the seven topologies are operated in d=0.73, their output voltage waveforms v_{R1} and inductor current waveforms i_{L1}~i_{L2} are the same. Similarly, the switch voltage waveform v_{S1} and diode voltage waveforms v_{D1}~v_{D2} are also the same among these seven topologies in Fig. 4(a)~(g). According above waveforms, experimental output voltage V_{R1}, switch voltage stress V_{S1}, and diode voltage stresses V_{D1}~V_{D2} are summarized in Fig. 3(h) and Fig. 4(h). It can be found that V_{R1} of seven topologies are all near 150V, satisfying the requirements. Besides, V_{S1}, V_{D1}, V_{D2}, I_{L1}, and I_{L2} are all near equal among the seven topologies, which agrees well with the fact that these converters with an equivalent CLC should have the similar performance.

Performance difference of these seven converters should be their capacitor voltages and their instantaneous currents. Taking topologies ①~② as example, their capacitor voltage waveforms v_{C1}~v_{C2} and input/output port waveforms i_{U1}, i_{R1} are shown in Fig. 5. It can be found that V_{C2} is 68V in topology ①, while 91V in topology ②. Besides, i_{R1} is discontinuous in topology ①, and continuous in topology ②. For further analysis, the input and output current waveforms of the seven converters are subjected to Fourier transformation, resulting in their amplitude frequency spectra in Fig. 6. With Fig. 6, it can be clearly observed that harmonic components of input/output currents may be different among these topologies. Notably, topologies ①~⑦ have equal 0Hz components of input/output currents in Fig. 6, which suggests they have equal average input/output currents.



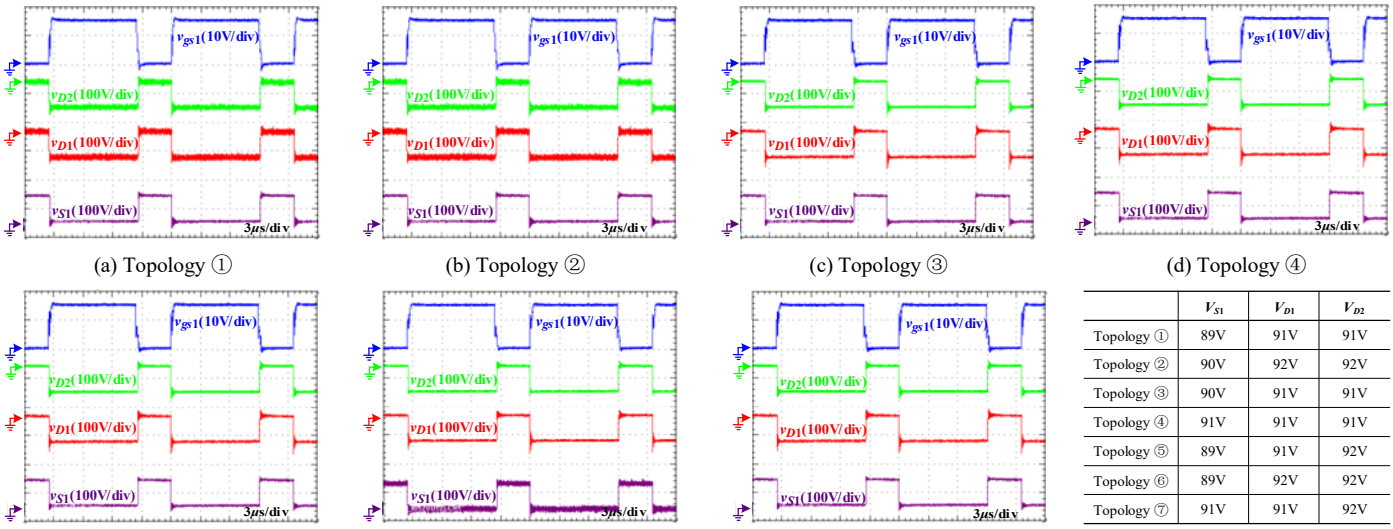
(a) Topology ① (b) Topology ② (c) Topology ③ (d) Topology ④

(e) Topology ⑤ (f) Topology ⑥ (g) Topology ⑦

	V_{R1}	I_{L1}	I_{L2}
Topology ①	148V	2.78A	0.40A
Topology ②	148V	2.77A	0.41A
Topology ③	148V	2.80A	0.41A
Topology ④	146V	2.78A	0.42A
Topology ⑤	147V	2.78A	0.43A
Topology ⑥	147V	2.80A	0.43A
Topology ⑦	146V	2.81A	0.41A

(h) Performance summary

Fig. 3. Waveforms of seven converters in Table IV, including drive signal v_{gs1}, output voltage v_{R1}, and inductor currents i_{L1}~i_{L2}.



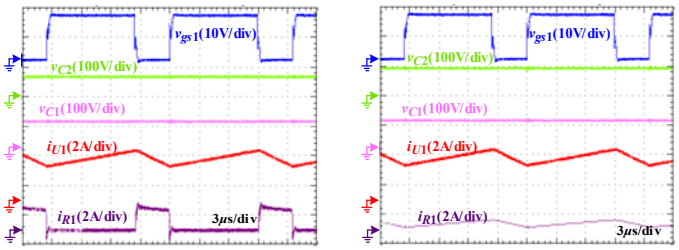
(a) Topology ① (b) Topology ② (c) Topology ③ (d) Topology ④

(e) Topology ⑤ (f) Topology ⑥ (g) Topology ⑦

	V_{S1}	V_{D1}	V_{D2}
Topology ①	89V	91V	91V
Topology ②	90V	92V	92V
Topology ③	90V	91V	91V
Topology ④	91V	91V	91V
Topology ⑤	89V	91V	92V
Topology ⑥	89V	92V	92V
Topology ⑦	91V	91V	92V

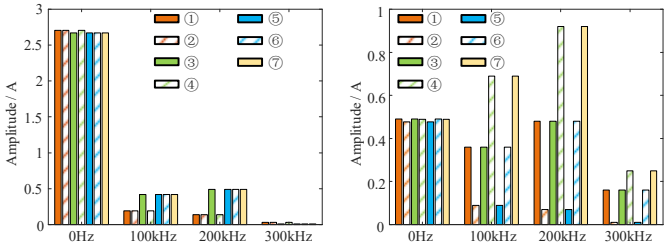
(h) Performance summary

Fig. 4. Waveforms of seven converters in Table IV, including drive signal v_{gs1}, switch voltage v_{S1}, and diode voltages v_{D1}~v_{D2}.



(a) Topology ① (b) Topology ②

Fig. 5. Waveform of topologies ①② in Table IV, including drive signal v_{gs1}, capacitor voltages v_{C1}~v_{C2}, and input/output port currents i_{U1}, i_{R1}



(a) Input current (b) Output current

Fig. 6. Amplitude-frequency plot of input/output currents of topologies ①~⑦.

VI. Conclusion

This letter reveals that Cuk, Sepic, and Zeta are three converters with capacitors connected in different positions of an equivalent CLC, and their equivalent CLCs lead to their similar performance characteristics. A novel topology derivation method based on CLC is proposed to derive families of converters with similar performance characteristics. In practical, CLC can be designed or extracted from existing converters, and the extracted CLC can be used to modify the existing converters to satisfy special requirements.

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