A MEMS Sensor Based on A Laterally Movable Gate Field-Effect Transistor (LMGFET) with A Novel Decoupling Sandwich Structure

Gao, Wendi; Qiao, Zhixia; Han, Xiangguang; Wang, Xiaozhang; Shakoor, Adnan; Liu, Cunlang; Lu, Dejiang; Yang, Ping; Zhao, Libo; Wang, Yonglu; Wang, Jiuhong; Jiang, Zhuangde; Sun, Dong

Published in: Engineering

Published: 01/02/2023

Document Version:
Final Published version, also known as Publisher's PDF, Publisher's Final version or Version of Record

License:
CC BY-NC-ND

Publication record in CityU Scholars:
Go to record

Published version (DOI):
10.1016/j.eng.2022.06.018

Publication details:

Citing this paper
Please note that where the full-text provided on CityU Scholars is the Post-print version (also known as Accepted Author Manuscript, Peer-reviewed or Author Final version), it may differ from the Final Published version. When citing, ensure that you check and use the publisher's definitive version for pagination and other details.

General rights
Copyright for the publications made accessible via the CityU Scholars portal is retained by the author(s) and/or other copyright owners and it is a condition of accessing these publications that users recognise and abide by the legal requirements associated with these rights. Users may not further distribute the material or use it for any profit-making activity or commercial gain.

Publisher permission
Permission for previously published items are in accordance with publisher's copyright policies sourced from the SHERPA RoMEO database. Links to full text versions (either Published or Post-print) are only available if corresponding publishers allow open access.

Take down policy
Contact lbscholars@cityu.edu.hk if you believe that this document breaches copyright and provide us with details. We will remove access to the work immediately and investigate your claim.
A MEMS Sensors Based on A Laterally Movable Gate Field-Effect Transistor (LMGFET) with A Novel Decoupling Sandwich Structure

Wendi Gao\textsuperscript{a,b,c}, Zhixia Qiao\textsuperscript{e}, Xiangguang Han\textsuperscript{a,b}, Xiaozhang Wang\textsuperscript{a,b}, Adnan Shakoor\textsuperscript{f,g}, Cunlang Liu\textsuperscript{a}, Dejiang Lu\textsuperscript{a,b,*}, Ping Yang\textsuperscript{a,b}, Libo Zhao\textsuperscript{a,b,*}, Yonglu Wang\textsuperscript{a,b}, Jiuhong Wang\textsuperscript{a,b}, Zhuangde Jiang\textsuperscript{a,b}, Dong Sun\textsuperscript{a,g}

\textsuperscript{a} State Key Laboratory for Manufacturing Systems Engineering, International Joint Laboratory for Micro/Nano Manufacturing and Measurement Technologies, Overseas Expertise Introduction Center for Micro/Nano Manufacturing and Nano Measurement Technologies Discipline Innovation, Xi'an Jiaotong University (Yantai) Research Institute for Intelligent Sensing Technology and System, School of Mechanical Engineering, Xi'an 710049, China
\textsuperscript{b} Expertise Introduction Center for Micro/Nano Manufacturing and Nano Measurement Technologies Discipline Innovation, Xi'an Jiaotong University (Yantai) Research Institute for Intelligent Sensing Technology and System, School of Mechanical Engineering, Xi'an 710049, China
\textsuperscript{c} State Key Laboratory of Robotics and Systems, Harbin Institute of Technology, Harbin 150006, China
\textsuperscript{d} Department of Biomedical Engineering, City University of Hong Kong, Hong Kong 999077, China
\textsuperscript{e} Beijing Advanced Innovation Center for Intelligent Robots and Systems, Beijing Institute of Technology, Beijing 100081, China
\textsuperscript{f} Shandong Laboratory of Yantai Advanced Materials and Green Manufacturing, Yantai 265503, China
\textsuperscript{g} Department of Control and Instrumentation Engineering, King Fahd University of Petroleum and Minerals, Dhahran 31261, Saudi Arabia
\textsuperscript{*}Department of Biomedical Engineering, City University of Hong Kong, Hong Kong 999077, China

ARTICLE INFO

Article history:
Received 3 September 2021
Revised 8 March 2022
Accepted 5 June 2022
Available online 13 August 2022

Keywords:
Force sensor
Laterally movable gate
Field-effect transistor
Photoresistive SU-8
Biomedical micromanipulation

ABSTRACT

This paper presents the development of a novel micro force sensor based on a laterally movable gate field-effect transistor (LMGFET). A precise electrical model is proposed for the performance evaluation of small-scale LMGFET devices and exhibits improved accuracy in comparison with previous models. A novel sandwich structure consisting of a gold cross-axis decoupling gate array layer and two soft photoresistive SU-8 layers is utilized. With the proposed dual-differential sensing configuration, the output current of the LMGFET lateral operation under vertical interference is largely eliminated, and the relative output error of the proposed sensor decreases from 4.53% (traditional differential configuration) to 0.01%. A practicable fabrication process is also developed and simulated for the proposed sensor. The proposed LMGFET-based force sensor exhibits a sensitivity of 4.65 \textmu A nN\textsuperscript{-1}, which is comparable with vertically movable gate field-effect transistor (VMGFET) devices, but has an improved nonlinearity of 0.78% and a larger measurement range of ±5.10 \textmu N. These analyses provide a comprehensive design optimization of the electrical and structural parameters of LMGFET devices and demonstrate the excellent force-sensing potential for biomedical micromanipulation applications.

© 2022 THE AUTHORS. Published by Elsevier LTD on behalf of Chinese Academy of Engineering and Higher Education Press Limited Company. This is an open access article under the CC BY-NC-ND license (http://creativecommons.org/licenses/by-nc-nd/4.0/).

1. Introduction

Micro-electromechanical system (MEMS) micro force sensors are efficient and necessary tools in many biomedical studies. Such tools have been used to measure the Young’s modulus [1,2], viscosity [3,4], and locomotion traction [5] in living cells or tissues in order to study biological processes and biomedical reactions. Micro force sensors can provide precise force feedback in micro-robotic biomedical manipulations to improve the automation extent [6,7] and the survival rate of biological objects [8,9]. Recent studies have focused on the organelle or molecular level, thereby increasing the demand for ultralow force sensing below the nanonewton level. Current force-sensing devices are mainly based on sensing principles, such as capacitive [10,11], piezoresistive [12,13], and piezoelectric [14,15] principles. The movable gate field-effect transistor (MGFET) force sensor exhibits several advantages over its competitors, such as a high sensitivity derived from the transistor array design [16,17], convenient signal amplification, and modulation with integrated circuits [18], thus making the on-chip measurement of low-scale forces feasible. Compared with traditional metal-oxide semiconductor field-effect transistors, MGFET devices have a floating gate over the substrate channel area and can move along three axes due to the air gap, as shown in Fig. 1. The current

https://doi.org/10.1016/j.eng.2022.06.018
2095-8099/© 2022 THE AUTHORS. Published by Elsevier LTD on behalf of Chinese Academy of Engineering and Higher Education Press Limited Company.
This is an open access article under the CC BY-NC-ND license (http://creativecommons.org/licenses/by-nc-nd/4.0/).
between the source and the drain electrodes reflects the applied external loads. In terms of the gate moving direction, MGFET devices are divided into two types: vertically MGFETs (VMGFETs) and laterally MGFETs (LMGFETs). VMGFETs exhibit high sensitivity, while their movement range is limited by the small air gap thickness. Their measurement linearity deteriorates with an increase in gate vertical deformation. Unexpected rapidly increased loads usually occur during biomedical measurements, such as during membrane penetration in biological cell microinjections [19,20], when the force amplitude increases sharply and may exceed the measurement range of a VMGFET device. In LMGFETs, the gate moves laterally along the channel width, and the air gap remains constant. The measurement range of LMGFETs is larger than that of VMGFETs, and their output current changes linearly during the measurement range. Therefore, a highly sensitive LMGFET force sensor is more versatile than a VMGFET in biomedical measurement.

Researchers have developed several MGFET devices on the basis of these two types, such as VMGFET-based accelerometers [21,22], differential amplifiers [23], and LMGFET-based displacement sensors [24]. Existing studies have found that the measuring sensitivity can be improved by scaling down the transistor size. However, the widely adopted long-channel model in Refs. [21–24], which ignores many scale effects, is inaccurate for describing MGFET performance, especially for devices with a small size. In our previous work, we proposed an accurate electrical model for small-scale VMGFET devices [25]. However, the movable gate of an LMGFET device partially covers the channel area, leaving the other part exposed. The operation behavior of LMGFET devices is relatively more complex than that of VMGFET devices, such that the previous VMGFET model is no longer applicable in LMGFET design. Therefore, a new precise electrical model is essential for the performance evaluation of small LMGFET devices. Moreover, the output current of an MGFET changes as its gate moves laterally and vertically, and loads from non-operation directions can produce considerable interference of output signals.

A differential sensing configuration has usually been adopted to attenuate the cross-axis coupling effect in MGFET devices [23,25]. However, this method is invalid for LMGFETs because the output current changes significantly when the gate moves vertically. The output change from lateral loads can be overwhelmed by vertical disturbances, producing undesirable measurement errors. Therefore, a novel decoupling movable structure and sensing configuration is required to improve sensing accuracy. The measuring sensitivity of MGFET devices can be further improved by lowering the stiffness of movable structures. In existing MGFET devices, movable structures are made of rigid materials, such as silicon [21] and nickel [22,24] with large stiffness, such that the movable structure can hardly deform. One feasible method to improve the measuring sensitivity is to replace these stiff materials with other flexible alternatives. However, this is difficult for LMGFET devices, as they require high-aspect-ratio structures, and such attempts have been conducted before.

The main contributions of this work are as follows. First, a separated channel-based electrical model is proposed to describe the operation behavior of small LMGFET devices, and its improved accuracy and capability for performance evaluation are demonstrated. Second, the electrical and structural parameters of LMGFET devices are fully analyzed to optimize the performance of ultralow force-sensing applications. Third, a flexible sandwich structure is proposed for the LMGFET micro force sensor, which consists of a gold cross-axis decoupling gate array layer and two soft photore sistive SU-8 layers. The sensor utilizes a novel dual-differential decoupling sensing configuration that exhibits excellent sensing sensitivity and anti-interference capability. Finally, the proposed LMGFET force sensor is simulated with a practicable fabrication process. The proposed sensor breaks through the limitation between the sensing accuracy and measurement range of MGFET devices. Its measuring sensitivity is 4.65 μA N−1 for a large measurement range of ±5.10 μN, and its nonlinearity is less than 0.78%.

The rest of this paper is organized as follows: Section 2 models and analyzes the electrical behavior of the LMGFET. Section 3 illustrates the proposed LMGFET force sensor and describes the mechanical model and sensing configuration. Section 4 presents a practicable fabrication process for the proposed sensor. The theoretical model is then validated through simulation and experimental results, followed by a discussion of the sensor performance. Section 5 provides the conclusions.

2. Electrical modeling of the LMGFET

When the gate of an LMGFET moves laterally, the channel width changes such that the LMGFET can be divided into two separated parts—namely, a covered channel area with width $W_{chu}$ and an uncovered channel area with width $W_{chu}$ ($W_{chu} = W_{ch} - W_{chc}$) (where $W_{ch}$ is the whole channel width). The two parts share some common parameters, such as the channel length $L_{ch}$, voltage difference between the gate and source electrode $V_{gs}$, and voltage difference between the drain and source electrode $V_{ds}$. Due to the difference in the gate modulation effect at different lateral positions, the electron conductance in each channel area differs significantly. The whole channel exhibits several individual electrical parameters, such as the gate capacitance $C_{gff}$, carrier mobility $\mu_{ff}$, and channel current $I_{ds}$. Thus, an investigation of the electrical parameters in each part is necessary in order to understand the operation principles of the LMGFET. Such an investigation is conducted in this section.

2.1. Effective gate capacitance

The capacitance between the gate and the covered and uncovered channel area changes when the gate moves laterally. Gate capacitance is a parameter describing the capacitance over a unit area. More specifically, the effective gate capacitance in the covered channel area $C_{eff}$ is the series capacitance of the air gap and gate insulator, which can be expressed as follows:

$$C_{eff} = \frac{e_0}{e_{INSu}} + Z_{air} = \frac{e_0}{Z_{eff}}$$

(1)

where $e_0 = 8.854 \times 10^{-14}$ F cm$^{-1}$ is the permittivity of air; $e_{INSu}$ is the permittivity of the insulator; $Z_{air}$ is the air gap thickness; $l_{INSu}$
is the insulator thickness; and \( Z_{\text{eff}} \) is the effective gate gap thickness in the covered area. A previous study assumed that the effective gate capacitance in the uncovered channel area \( C_{\text{eff}} \) is constant during gate movement [24]; however, this assumption is not in accordance with reality and can cause many artifacts in the device performance estimation. In this study, we propose an accurate variable expression of \( C_{\text{eff}} \) based on the fringe parasitic effect of the gate sidewall and bottom line [26,27]:

\[
C_{\text{eff}} = \frac{2 \varepsilon_0}{\pi W_{\text{chu}}} \ln \left( \frac{Z_{\text{eff}} + T_g + \sqrt{T_g^2 + 2T_g'Z_{\text{eff}}}}{Z_{\text{eff}}} \right) + \frac{k_0}{\pi W_{\text{chu}} L_{\text{ch}}} \ln \left( \frac{\pi L_{\text{ch}}}{Z_{\text{eff}}} \right)
\]

\[
= \frac{\varepsilon_0}{Z_{\text{eff}}} \left( \frac{\pi W_{\text{chu}} - \sqrt{T_g^2 + 2T_g'Z_{\text{eff}}}}{\beta Z_{\text{eff}}} \right)
\]

where \( T_g = T_{\text{eff}} e \) is the effective gate thickness for the sidewall parasitic capacitance; \( T_g \) is the gate thickness; \( k \) and \( \beta \) are fitting parameters; and \( Z_{\text{eff}} \) is the effective gate gap thickness in the uncovered area.

The effective gate capacitance of the two separated areas is examined at different lateral and height positions and compared with simulation results from the finite-element method (FEM) software Ansoft Maxwell. In this calculation, the whole channel width \( W_{\text{ch}} \) is 20 \( \mu \)m; the air gap thickness \( Z_{\text{chu}} \) is from 0.1 to 0.5 \( \mu \)m; the gate thickness \( T_{\text{eff}} \) is 0.2 \( \mu \)m; the gate insulator is silicon nitride, and its thickness \( T_{\text{nms}} \) is 100 \( \mu \)m; and the channel length \( L_{\text{ch}} \) is 5 \( \mu \)m. During gate movement, most of the electric potential is concentrated in the covered area, and a small amount is scattered on the boundary edge because of the fringe parasitic effect. The effective gate capacitance in the covered channel area \( C_{\text{eff}} \) remains almost constant at full width. As the covered area width \( W_{\text{chu}} \) approaches zero, the scattered potential proportion increases, and \( C_{\text{eff}} \) experiences a small increase, as shown by the dots in Fig. 2. However, the relative error of \( C_{\text{eff}} \) between the model and the simulation results is less than 3.0% for a small \( W_{\text{chu}} \) of 1 \( \mu \)m in three different air gaps. The value of the effective gate capacitance in the uncovered channel area \( C_{\text{eff}} \) is one order less than that of \( C_{\text{eff}} \). The gate capacitance in the uncovered area mainly results from the scattered electric potential in the gate sidewall and bottom line. The total electrical potential remains constant, but the size of the uncovered area changes during gate movement. \( C_{\text{eff}} \) exhibits an inversely proportional relationship with width in the covered area \( W_{\text{chu}} \). When \( W_{\text{chu}} \) is low, \( C_{\text{eff}} \) increases slowly because the change in \( W_{\text{chu}} \) is insigniﬁcant. However, the size of the uncovered area changes greatly as \( W_{\text{chu}} \) approaches the whole channel width, resulting in a rapid increase of \( C_{\text{eff}} \). The scattered electrical potential increases as the air gap \( Z_{\text{air}} \) decreases and then aggravates this phenomenon. The calculation of \( C_{\text{eff}} \) also shows an excellent coincidence with the simulated results, where the largest relative error is less than 3.5%.

### 2.2. Threshold voltage

Threshold voltage is a crucial switch parameter modulating the current channel between the source and drain electrodes. The channel current exists only if the gate voltage is larger than the threshold voltage for an accumulation-type MGFET. For a depletion-type device, in which the channel current is originally induced, a gate voltage approaching the threshold value can break off the conducting channel. The covered and uncovered channel areas have different threshold voltages, so they can have different channel statuses during lateral and vertical gate movement. Considering the short and narrow channel effects, the threshold voltages in the two areas are modeled separately, as follows:

\[
V_{\text{thc}} = \varphi_{\text{BS}} + \varphi_{\text{B}} \pm F_g \frac{Z_{\text{eff}} \sqrt{2qN_a/d_{\text{chu}}(\varphi_{\text{B}} - V_{\text{bs}})}}{e_0} + Q_{\text{eff}} Z_{\text{eff}} \frac{e_0}{Z_{\text{eff}}}
\]

\[
V_{\text{thu}} = \varphi_{\text{BS}} + \varphi_{\text{B}} \pm F_g \frac{Z_{\text{eff}} \sqrt{2qN_a/d_{\text{chu}}(\varphi_{\text{B}} - V_{\text{bs}})}}{e_0} + Q_{\text{eff}} Z_{\text{eff}} \frac{e_0}{Z_{\text{eff}}}
\]

where \( \varphi_{\text{BS}} \) is the work function difference between the gate and channel; \( \varphi_{\text{B}} \) is the channel built-in voltage, which is \( \frac{k_0 T}{q} \ln \left( \frac{N_a}{n_i^2} \right) \) and \( \frac{k_0 T}{q} \ln \left( \frac{N_d}{n_i^2} \right) \) for an N-channel device and a P-channel device, respectively; \( N_{a/d} \) is the net concentration of ionized acceptors in a P-type substrate and donors in an N-type substrate, respectively; \( q = 1.6 \times 10^{-19} \) C is the magnitude of the electron or hole charge, \( n_i \) is the intrinsic doping concentration of silicon, \( k_b \) is the Boltzmann constant, and \( T \) is the thermodynamic temperature; \( e_0 \) is the permittivity of silicon; \( V_{\text{bs}} \) is the voltage difference between the source and substrate electrodes; \( Q_{\text{eff}} \) is the effective charge density of the channel, where the minus and plus signs are respectively for N-channel and P-channel devices; and \( F_g \) is the channel length coefficient, which is expressed as follows:

\[
F_g = 1 - \frac{d_1}{L_{\text{ch}}} \left[ a + d_0 + d_1 \sqrt{\frac{2x_i(\varphi_{\text{B}} - V_{\text{bs}})}{x_i}} \right] + d_2 \left( \frac{\sqrt{2x_i(\varphi_{\text{B}} - V_{\text{bs}})}}{x_i} \right)^2
\]

\[
\times \left[ 1 - \left( \frac{\sqrt{2x_i(\varphi_{\text{B}} - V_{\text{bs}})}}{x_i} \right) \right] - \frac{\alpha X_i}{L_{\text{ch}}}
\]

where \( X_i \) is the depth of the P–N junctions in the source or the drain electrode; and \( d_1, d_2, d_3, d_4, \) and \( d_5 \) are model parameters. \( F_{\text{NC}} \) and \( F_{\text{NT}} \) are the channel width coefficients in the covered and uncovered channel areas, respectively, and are expressed as follows:

\[
F_{\text{NC}} = \frac{\delta \pi W_{\text{chu}} Z_{\text{eff}}}{4W_{\text{chu}} L_{\text{ch}} e_0}
\]
\[ F_{\text{th}(a)} = \frac{\delta \pi \varepsilon_{0} Z_{\text{eff}}}{4 W_{\text{th}} V_{\text{th}}(0)} \] (7)

where \( \delta \) is the channel width model factor. The positive sign before the \( F_{\text{th}} \) term is for an N-channel device while negative sign is for a P-channel device. The sign before the \( Q_{\text{eff}} \) term is opposite compared with that before the \( F_{\text{th}} \) term, and the difference between the \( F_{\text{th}} \) and the \( Q_{\text{eff}} \) term can primarily determine the value of the threshold voltage. For example, a large \( Q_{\text{eff}} \) term can result in a negative threshold voltage for a depletion-type MGFET device with a P-type substrate (Fig. 3).

Although the channel length coefficient \( F_{\text{th}} \) remains constant, the channel width coefficient changes during lateral and vertical gate movements, especially for the uncovered channel area, whose effective gate gap \( Z_{\text{eff}} \) varies significantly at different positions. Therefore, the threshold voltage will exhibit different characteristics in the two channel areas and needs comprehensive analysis. The effective charge density of the channel \( Q_{\text{eff}} \) and the substrate concentration \( N_{\text{id}} \) are studied first. A P-type substrate device is adopted as an example, with the following parameters: The channel width \( W_{\text{th}} \) is 20 \( \mu \text{m} \), the air gap \( Z_{\text{air}} \) is 0.25 \( \mu \text{m} \), the channel length \( l_{\text{ch}} \) is 5 \( \mu \text{m} \), the P-N junction depth \( X_{\text{p}} \) is 0.5 \( \mu \text{m} \), the intrinsic doping concentration \( n_{\text{i}} \) is \( 1.5 \times 10^{16} \text{cm}^{-3} \), the implanted model constant \( a = 0.04 \), \( d_{\text{a}} = 0.6031353 \), \( d_{\text{b}} = 0.8013292 \), \( d_{\text{c}} = 0.01110777 \), the work function voltage difference \( \phi_{\text{MS}} \) is 3.83 \( V \), and the voltage difference between the substrate and the source electrode \( V_{\text{th}} \) = 0 \( V \). The remaining parameters are the same as those given in Section 2.1. The effect of the substrate acceptor concentration \( N_{\text{s}} \) is investigated from Case_1 to Case_4 in Table 1, where \( N_{\text{s}} \) increases from \( 5 \times 10^{14} \) to \( 5 \times 10^{15} \text{cm}^{-3} \) while \( Q_{\text{eff}} \) is kept low at \( 2.5 \times 10^{-8} \text{cm}^{-2} \). For a small \( N_{\text{s}} \) in Case_1, both parts behave as depletion-type transistors, and the channel is initially conductive because their energy band has been bent by dominant electrons in the channel surface. To break off the conducting channel, a negative threshold voltage is required to attract holes in the channel surface. To break off the conducting channel, a negative threshold voltage is required to attract holes in the channel surface. However, \( V_{\text{thu}} \) becomes positive while \( V_{\text{th}} \) remains negative when \( N_{\text{s}} \) increases to 1.0 \( \times 10^{15} \text{cm}^{-3} \), the covered part becomes an accumulation-type transistor, and the uncovered part remains a depletion type in Case_2. Because of its flat energy band, the channel in the covered area is not conductive until the inversion layer is formed, wherein holes gather in the channel surface under electrical potential forces resulting from a positive threshold voltage \( V_{\text{thc}} \). This condition appears to be desirable for device design, because the uncovered part with a nonlinear effective gate capacitance can be eliminated. However, it results in poor device performance, as only the covered part contributes to the output current.

During LMGFET operation, \( V_{\text{thc}} \) decreases moderately and \( V_{\text{th}} \) increases sharply as \( W_{\text{th}} \) increases, indicating that \( V_{\text{th}} \) is more susceptible to channel width modulation. More specifically, \( V_{\text{thu}} \) changes from \(-0.817 \text{V} \) at a \( W_{\text{th}} \) of 13 \( \mu \text{m} \) to 0.074 \( V \) at a \( W_{\text{th}} \) of 14 \( \mu \text{m} \) in Case_3. This condition can make the uncovered area change from a depletion type to an accumulation type during operation and should be avoided. When \( N_{\text{s}} \) increases above \( 5 \times 10^{15} \text{cm}^{-3} \), the two areas become accumulation types in Case_4. The effect of the channel's effective charge density \( Q_{\text{eff}} \) is then investigated from Case_5 to Case_8, where \( Q_{\text{eff}} \) increases from \( 1 \times 10^{-8} \text{cm}^{-2} \) to \( 3 \times 10^{-7} \text{cm}^{-2} \). In these cases, \( N_{\text{s}} \) is kept at \( 5 \times 10^{15} \text{cm}^{-3} \), a value that is commonly available using commercial silicon wafers. For a low \( Q_{\text{eff}} \) of \( 1 \times 10^{-8} \text{cm}^{-2} \) in Case_5, the covered part behaves as an accumulation-type transistor, while the uncovered part is a depletion type. Holes become dominant as \( Q_{\text{eff}} \) increases from \( 1 \times 10^{-8} \) to \( 3 \times 10^{-7} \text{cm}^{-2} \), while \( N_{\text{s}} \) is kept at \( 1 \times 10^{15} \text{cm}^{-3} \). The effect of the channel's effective charge density \( Q_{\text{eff}} \) is then investigated from Case_5 to Case_8, where \( Q_{\text{eff}} \) increases from \( 1 \times 10^{-8} \text{cm}^{-2} \) to \( 3 \times 10^{-7} \text{cm}^{-2} \). In these cases, \( N_{\text{s}} \) is kept at \( 5 \times 10^{15} \text{cm}^{-3} \), a value that is commonly available using commercial silicon wafers. For a low \( Q_{\text{eff}} \) of \( 1 \times 10^{-8} \text{cm}^{-2} \) in Case_5, the covered part behaves as an accumulation-type transistor, while the uncovered part is a depletion type. Holes become dominant as \( Q_{\text{eff}} \) increases from \( 1 \times 10^{-8} \) to \( 3 \times 10^{-7} \text{cm}^{-2} \), while \( N_{\text{s}} \) is kept at \( 1 \times 10^{15} \text{cm}^{-3} \).

**Table 1** Threshold voltage of covered/uncovered channel area under different electrical parameters.

<table>
<thead>
<tr>
<th>Case</th>
<th>( N_{\text{s}} ) (cm(^{-2}))</th>
<th>( Q_{\text{eff}} ) (C cm(^{-2}))</th>
<th>( V_{\text{thu}} ) (V)(^a)</th>
<th>( V_{\text{th}} ) (V)(^b)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( 5 \times 10^{14} )</td>
<td>( 2.5 \times 10^{-8} )</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>2</td>
<td>( 1 \times 10^{15} )</td>
<td>( 2.5 \times 10^{-8} )</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>( 3 \times 10^{15} )</td>
<td>( 2.5 \times 10^{-8} )</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>( 5 \times 10^{15} )</td>
<td>( 2.5 \times 10^{-8} )</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>5</td>
<td>( 1 \times 10^{15} )</td>
<td>( 1.0 \times 10^{-8} )</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>6</td>
<td>( 1 \times 10^{15} )</td>
<td>( 5.0 \times 10^{-8} )</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>7</td>
<td>( 1 \times 10^{15} )</td>
<td>( 1.0 \times 10^{-7} )</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>8</td>
<td>( 1 \times 10^{15} )</td>
<td>( 3.0 \times 10^{-7} )</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>

\(^a\)"+" and "-" refer to accumulation and depletion types, respectively.

\(^b\)"-/+" indicates that the device changes from a depletion to accumulation type.

**Fig. 3.** Relationship between the threshold voltages \( V_{\text{th}(a)} \) and \( V_{\text{th}(b)} \) and electrical parameters at different width positions. (a) Net concentration of ionized acceptors in the substrate \( N_{\text{s}} \); (b) effective channel charge density \( Q_{\text{eff}} \). Symbol lines indicate the threshold voltage in the covered channel area \( V_{\text{th}(a)} \), and dotted lines indicate the threshold voltage in the covered channel area \( V_{\text{th}(b)} \). Case_1–Case_4: \( N_{\text{s}} \) increases from \( 5 \times 10^{14} \) to \( 5 \times 10^{15} \text{cm}^{-3} \), while \( Q_{\text{eff}} \) is kept low at \( 2.5 \times 10^{-8} \text{cm}^{-2} \). Case_5–Case_8: \( Q_{\text{eff}} \) increases from \( 1 \times 10^{-8} \) to \( 3 \times 10^{-7} \text{cm}^{-2} \), while \( N_{\text{s}} \) is kept at \( 1 \times 10^{15} \text{cm}^{-3} \).
increases above $5 \times 10^{-4}$ C cm$^{-2}$, allowing both areas to function as depletion-type transistors.

The relationship between the threshold voltage $V_{th}$ and the geometry parameters $L_{ch}$ and $Z_{air}$ is shown in Fig. 4, where $N_A$ and $Q_{eff}$ are set at $1 \times 10^{14}$ cm$^{-3}$ and $2.5 \times 10^{-7}$ C cm$^{-2}$, respectively. $V_{thc}$ has a strong negative correlation with the air gap $Z_{air}$ as the effective gate height $Z_{eff}$ increases. However, $V_{thc}$ rarely changes for different channel lengths $L_{ch}$. $V_{thu}$ increases slowly with an increase in channel length $L_{ch}$, but decreases significantly with an increase in the air gap $Z_{air}$ for the same reason as $V_{thc}$. Therefore, the desired working types are achievable through appropriate assignment of electrical and geometry parameters. A nonzero gate voltage inducing a conducting channel in an accumulation-type device can probably produce an electrostatic force between the movable gate and substrate, resulting in undesirable vertical interference during operation [28]. The channel of a depletion-type device is conducted, although the potential difference is zero. Thus, electrostatic forces are eliminated. In other words, a depletion type is strongly expected for LMGFET devices. Therefore, the following design analysis is based on the norm that an LMGFET is free from electrostatic forces with a fixed gate voltage of 0 V.

### 2.3. Output channel current

The surface current density in two channel areas differs from each other. Thus, the current between the drain and source electrode in each area should be calculated individually, and the total output current should be their sum. By integrating the density of the channel surface carriers between two electrodes [29], the output current in the covered area $I_{dsu}$ and the output current in the uncovered area $I_{dsu}$ are defined as follows:

$$I_{dsu} = \frac{W_{ch} \mu_{eff} Z_{eff} Z_{air}}{L_{ch} \delta_0} \left( V_{gs} - V_{thc} - \frac{1 + F_{Bc} \theta}{2} V_{ds} \right) V_{ds}$$

$$I_{dsu} = \frac{W_{ch} \mu_{eff} Z_{eff} Z_{air}}{L_{ch} \delta_0} \left( V_{gs} - V_{thu} - \frac{1 + F_{Bu} \theta}{2} V_{ds} \right) V_{ds}$$

where $F_{Bc/u} = F_{SL} \sqrt{2 Q_{eff} / (\phi_A - V_{gs}))} + F_{NC/u}$ is a voltage modulation coefficient in the covered and uncovered areas; $\mu_{eff}$ and $\mu_{eff}$ are the effective carrier mobilities in the covered and uncovered areas, respectively, which can be expressed as follows:

$$\mu_{eff} = \frac{\mu_0}{1 + \frac{\delta}{Z_{eff}} (V_{gs} - V_{thc}) + \frac{\theta}{V_{max,ch}} V_{ds}}$$

$$\mu_{eff} = \frac{\mu_0}{1 + \frac{\delta}{Z_{eff}} (V_{gs} - V_{thu}) + \frac{\theta}{V_{max,du}} V_{ds}}$$

where $\mu_0$ is the surface mobility of the carriers at a low electric field; $\delta$ is the vertical potential field factor; and $V_{max}$ is the saturated velocity of the carriers. Effective carrier mobility is mainly regulated by the term $\frac{\delta}{Z_{eff}} (V_{gs} - V_{thu,v})$, which accounts for the vertical potential degrading effect, and by the term $\frac{\theta}{V_{max,du}} V_{ds}$, which describes the velocity limitation and lateral potential degrading effect [30]. $\mu_{eff}$ and $\mu_{eff}$ change when the gate shifts to different channel widths and heights. $I_{ds}$ approaches the value of the saturated current $I_{sat}$ when $V_{gs}$ increases to a saturated status.

As discussed in our previous work [25], the saturated voltage of small-scale devices results from a saturated velocity. The saturated voltages in the covered area $V_{dsat}$ and in the uncovered channel $V_{dsatu}$ are expressed as follows:

$$V_{dsat} = \frac{V_{gs} - V_{thc}}{1 + F_{Bc}} - \frac{V_{max,ch}}{\mu_{eff}} - \left( \frac{V_{gs} - V_{thc}}{1 + F_{Bc}} \right)^2 - \left( \frac{V_{max,ch}}{\mu_{eff}} \right)^2$$

$$V_{dsatu} = \frac{V_{gs} - V_{thu}}{1 + F_{Bu}} - \frac{V_{max,du}}{\mu_{eff}} - \left( \frac{V_{gs} - V_{thu}}{1 + F_{Bu}} \right)^2 - \left( \frac{V_{max,du}}{\mu_{eff}} \right)^2$$

where $I_{dsat}$ is the maximum controllable output for LMGFET devices and is directly affected by the threshold voltage applied at the drain electrode. Fig. 5 illustrates the relationship between the threshold voltage in the two areas and the electrical parameters (with acceptor concentration $N_A$ and effective channel charge density $Q_{eff}$) and geometrical parameters (with air gap $Z_{air}$ and channel length $L_{ch}$). Aside from the similar parameters in the last calculation, the voltage difference between the substrate and source electrode $V_{gs}$ is 0 V, the carrier surface mobility $\mu_0$ is 700 cm$^2$ V$^{-1}$ s$^{-1}$ [31], and the saturated velocity $V_{max}$ is $8 \times 10^4$ cm s$^{-1}$ [32]. The saturated voltages of the two areas decrease with an increase in $N_A$ and $Q_{eff}$; they also decrease with a decrease in the corresponding channel width ($W_{ch}$/$W_{ch}+u$). More specifically, the decreasing amplitude due to a small width becomes distinct with an increase in $N_A$ and $Q_{eff}$. The green lines in Fig. 5(a) correspond to Case_2 in Table 1. The covered channel area is currently broken off, so the saturated voltage in the covered area is 0. The geometric parameters exhibit an opposite influence to the electrical ones. $V_{dsat}$ increases with an increase in $L_{ch}$ and $Z_{air}$, as shown in Fig. 5(b). $V_{dsatu}$ increases with an increase in $L_{ch}$ and is insensitive to the change in the air gap $Z_{air}$. For a channel width $W_{ch}$ of 10 $\mu$m, $V_{dsatu}$ only changes by 0.18 V when $Z_{air}$ changes from 0.1 to 0.5 $\mu$m.

The adopted saturated voltage is set to the lowest value during the gate's lateral movement to analyze the saturated current. The current $I_{gs}$ is assumed to be constant if the applied voltage exceeds the saturated value in each area. A large $Q_{eff}$ or lower $N_A$ results in a large $I_{dsat}$ in two areas due to the large absolute value of the threshold voltages $V_{dsat}$ and $V_{dsatu}$. The saturated current is approximately zero when only the uncovered channel works in this case, as shown by the green lines of Fig. 6(a). The deformation sensitivity

![Fig. 4. Relationship between the threshold voltage $V_{th}$ and the geometry parameters $L_{ch}$ and $Z_{air}$ at different width positions.](image-url)
S is defined as the slope of the channel current curves and can be used to evaluate the electrical performance of the device when the gate moves laterally. The sensitivity $S$ improves with an increase in the channel length $L_{\text{ch}}$. For an air gap $Z_{\text{air}}$ of 0.25 µm, $S$ increases from 13.144 to 17.140 A/Cm when $L_{\text{ch}}$ decreases from 10 to 2 µm. However, the device operation stability should be considered, because a small device size can result in a large potential field between the drain and source electrode and can easily break down the device. The air gap $Z_{\text{air}}$ has a very large effect on the channel current $I_{\text{ds}}$ and sensitivity $S$. For the device with a channel width $W_{\text{ch}}$ of 10 µm and a channel length of 5 µm, the channel current $I_{\text{ds}}$ increases from 1509.744 to 1796.400 A when $Z_{\text{air}}$ decreases from 0.5 to 0.1 µm. However, $S$ decreases from 34.634 to 8.314 A/Cm during this period, as shown in Fig. 6(b). This condition indicates that the output produced from undesirable vertical movement can be several times greater the current change from lateral movement. Therefore, a decoupling design is required to eliminate the interference from vertical movement, as discussed in the next section.

3. Sensor design and interconnection configuration

The proposed sensor utilizes an epoxy-type polymer photore sist, SU-8, as the structural material, which is an ideal material to fabricate LMGFET devices for the following reasons: First, SU-8 has a relatively low elastic modulus of 4–5 GPa, high mechanical strength, and stable chemical stability after ultraviolet (UV) exposure [33,34]. Second, SU-8 is a negative thick-film photoresist and can be used fabricate structures with a high aspect ratio [35]. These features make SU-8 suitable to serve as the structural material of laterally movable structures. Third, it is easy to uniformly deposit SU-8 on the substrate by utilizing a spin-coater or spray-coater, even for unleveled surfaces [36]. Finally, SU-8 can be easily patterned by UV exposure and developed in a propylene glycol methyl ether acetate solution, which is very much considerably more operable than etching materials, such as metal and silicon. In this research, an SU-8-based LMGFET force sensor with a movable sandwich structure is proposed, as discussed in the following section.

3.1. Movable structure design

The movable structure and the substrate are two main components in the device, as shown in Fig. 7(a). The movable structure contains a probe and a center mass supported by straight beams. Fig. 7(b) shows the sandwich gate structure in which a gold gate electrode layer is fully covered by two photoresistive SU-8 layers. Gold is a common metal material in most labs and has been demonstrated to have excellent adhesion to SU-8 [37]. The thickness of the lower SU-8 structural layer should be small in order to decrease the effective gate gap and effective capacitance. Two series of gold gate arrays, $S_1$ and $S_2$, are set in the center mass with an offset distance $D_{\text{off}}$. In each series, two gate arrays lie symmetrically about with respect to the lateral lines Line_1 and Line_2. The gates in two series have the same width $W_g$ and length $L_g$. The corresponding drain, source electrodes, and gate insulator layer are positioned underneath the gate arrays. The channel region has width $W_{\text{ch}}$ and length $L_{\text{ch}}$ and lies between the drain and the source electrode. In the initial state, the gate covers half of the channel width, as shown in Fig. 7(c).

When a lateral force $F_Y$ is applied at the probe, the beams are involved in bending deformation. The gate arrays in the center mass move laterally and change the width of the channel area, which is expressed as follows:

$$W_{\text{ds}} = \frac{F_Y l_g^2}{48E l_f}$$

(14)
where $W_{fy}$ is the structure deformation along $Y$-axis under $F_Y$; $E$ is the Young’s modulus of the structural materials; $I_Y = \frac{W_b T_b^3}{12}$ is the moment inertia of the beam vertical section; and $L_{b}$, $W_{b}$, and $T_{b}$ are the length, width, and thickness of the supporting beam, respectively. When a vertical force $F_Z$ is applied, the structure experiences a vertical force applied at mass center $F_0$ and a force-induced moment $M_X = \frac{F_Z (L_p + \frac{1}{2} L_m)}{24EI_z}$ (where $L_p$ is the probe length and $L_m$ is the center mass length), which involve a vertical translation $Z_F$ and a rotation around the X-axis for mass $\theta_X$, as shown in Fig. 8; their expressions are

$$Z_F = \frac{F_Z L_p^3}{48EL_z}$$  \hspace{1cm} (15)

$$\theta_X = \frac{M_X L_m^3}{24EI_z (L_m - L_p)}$$  \hspace{1cm} (16)

where $I_z = \frac{W_b T_b^3}{12}$ is the moment inertia of the beam horizontal section. On this basis, a line with a distance of $D_{off}$ exists away from the mass center line and has zero vertical displacement. This line is expressed as follows:

$$D_{off} = \frac{L_m - L_p}{2L_p + L_m}$$  \hspace{1cm} (17)

The vertical displacement of the gate series from force $F_Z$ is expressed as follows:
deformation ratio \( r \) is 1964, demonstrating the low cross-axis coupling effect in this structure.

### 3.2. Sensing configuration

Although the proposed structure rarely undergoes cross-axis deformation, undesired vertical deformation will inevitably bring interference to the channel current. Aside from the decoupling movable structure design, a sensing configuration is required to eliminate the cross-axis output coupling. A differential sensing configuration is normally adopted to compensate for loads from non-operation directions and for external disturbances, such as temperature and humidity. However, this method is unsuitable for LMIGFET sensing because vertical movement of gate arrays different according to their position. In this research, a novel dual-differential sensing configuration is proposed, in which the underlying channel region is not aligned with the gate arrays but is distributed anti-symmetrically about the center of Line_1 and Line_2, as shown in Fig. 10. Each transistor series is separated into four arrays: S1LU, S1LD, S1RU, and S1RD are for series S1, while S2LU, S2LD, S2RU, and S2RD are for series S2. The interconnection configurations of S1 and S2 are illustrated in Figs. 11(a) and (b), respectively. S2 is for lateral force detection, and S1 is for vertical force detection. This paper focuses on lateral force detection. Thus, the following description is conducted with series S2. \( I_{dL} \) is the sum of the current of two left transistor series S2LU and S2LD, and \( I_{dR} \) is the sum of the current of two right transistor series S2RU and S2RD. These expressions can be written as follows:

\[
I_{dL} = I_{dL1} (W_{chc} + W_{ff}, Z_{air} + Z_{f}) + I_{dL2} (W_{chc} + W_{ff}, Z_{air} - Z_{f})
\]

\[
I_{dR} = I_{dR1} (W_{chc} + W_{ff}, Z_{air} + Z_{f}) + I_{dR4} (W_{chc} + W_{ff}, Z_{air} - Z_{f})
\]

where \( I_{dL1}, I_{dL2}, I_{dR3}, \) and \( I_{dR4} \) are the current of the transistor series S2LU, S2LD, S2RU, S2RD, respectively.

Most vertical interferences are counteracted in Eqs. (20) and (21). The final sensor output can be measured with the potential difference between two circuit branches, \( V_{out} = R \times (I_{dL} - I_{dR}) \) (where \( R \) is the connected resistor in the readout circuit). The sensing performance of the proposed dual-differential configuration is illustrated in Fig. 12, and it is compared with the normal differential method, where the channel region is aligned with the gate array. The difference between the initial output and that under the vertical displacement is measured with relative errors for the two methods, as shown in Figs. 12(a) and (b).

For a 1 nN force loaded in the sensor probe, the sandwich structure moves 1.961 nm laterally but 0.001 nm vertically. Therefore, the vertical displacement is set from 0.001 to 3.000 nm in order to investigate the sensing performance under vertical forces ranging from 1 nN to 3 \( \mu \)N. The relative errors of the two methods are negligible for a small vertical displacement of less than 0.03 nm. Because of the rapid increased \( C_{eff} \), the relative error of the differential channel current increases until \( W_{chc} \) reaches 7.5 \( \mu \)m. The relative error of the normal differential method at \( V_{dss} \) reaches 4.53% for a 3 nm vertical displacement, and that of the proposed method is less than 0.01%. When \( W_{chc} \) reaches 10 \( \mu \)m, the relative errors solely resulting from the covered area exhibit a drop because \( C_{eff} \) disappears.

### Table 2

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Young’s modulus of SU-8 photoresist</td>
<td>4.4 GPa</td>
</tr>
<tr>
<td>Poisson’s ratio of SU-8 photoresist</td>
<td>0.22</td>
</tr>
<tr>
<td>Thickness of lower SU-8 structure layer</td>
<td>0.5 ( \mu )m</td>
</tr>
<tr>
<td>Thickness of upper SU-8 structure layer</td>
<td>49.5 ( \mu )m</td>
</tr>
<tr>
<td>Air gap ( Z_{gap} )</td>
<td>0.1 ( \mu )m</td>
</tr>
<tr>
<td>Length of center mass ( L_{m} )</td>
<td>2000 ( \mu )m</td>
</tr>
<tr>
<td>Width of center mass ( W_{m} )</td>
<td>1700 ( \mu )m</td>
</tr>
<tr>
<td>Length of gate ( L_{g} )</td>
<td>20 ( \mu )m</td>
</tr>
</tbody>
</table>
deformation behavior of the movable structure, a 3 nm vertical deformation of the gate series S1 demands a vertical force of 3 μN. The gate series cannot deform at 3 nm because the mass end face could touch the substrate under vertical forces below such a value. Therefore, the cross-axis coupling effect is thoroughly eliminated in the proposed dual-differential sensing configuration.

4. Model validation and sensor performance

4.1. Fabrication process

A simple but practicable fabrication is proposed for the presented LMGFET device, as shown in Fig. 13. A photoresist layer is deposited and patterned to define the drain and source electrode and its interconnections; the substrate is then ion-implanted to form phosphorus-doped areas. Through another patterned photoresistive layer, the channel area is defined and then doped with phosphorus ions but using different implantation doses and...
The implanted ions are activated through rapid thermal annealing. A gate insulation layer made of silicon nitride is deposited and then patterned to expose contact holes for source/drain interconnections. Subsequently, a sacrificial layer of silicon dioxide is deposited and patterned to expose the structure anchors and contact holes. A thin SU-8 structural layer is spun, exposed, and developed to act as the lower layer of the sandwich structure. A gold layer is then deposited and patterned to act as the gate arrays and pads of the drain and source electrodes. The substrate metal pad is formed through another gold layer deposited on the bottom side of the chip. Another thick SU-8 layer is spun to seal the gate array and is patterned for the upper sandwich structural layer. The substrate is patterned with deep reactive ion etching to expose the probe area. Finally, isotropic etching of the sacrificial silicon dioxide layer is conducted to release the movable sandwich structure.

The fabrication process is simulated using FEM Software Sonatas 13.0; the adopted parameters are illustrated in Table 3 and the simulated LMGFET unit is shown in Fig. 14(a). The device is modeled as a single transistor to simplify the computation complexity, and the air gap and lower SU-8 structural layer are replaced with an effective silicon dioxide layer $T_{\text{SiO}_2}$ by using the following expression:

$$T_{\text{SiO}_2} = \frac{\varepsilon_{\text{SiO}_2} Z_{\text{air}}}{\varepsilon_0} + \frac{\varepsilon_{\text{SiO}_2} T_{\text{low-SU-8}}}{\varepsilon_{\text{SU-8}}}$$  \hfill (22)
where $T_{\text{low-SU-8}}$ and $\varepsilon_{\text{SU-8}}$ are the thickness and permittivity of the lower SU-8 layer, and $\varepsilon_{\text{SiO2}}$ is the permittivity of silicon dioxide. The peak implanted ion concentration in the channel area is $1 \times 10^{17} \text{ cm}^{-2}$, which is achievable in the bath fabrication process as discussed in our previous work [25]. The characteristic of how the distribution of channel impurities influences the channel current is investigated by setting different ion implantation depths from 0.150 to 0.300 µm. Fig. 14(b) shows a cross-section view of the activated implanted phosphorous distribution at an implantation depth of 0.275 µm. The inset shows the extracted concentration profile of active phosphorus in the channel region for the device in Fig. 14(a). A rectangular approximation is modeled to describe the concentration profile, as shown by the read dotted line in Fig. 14(b). The effective channel charge density $Q_{\text{eff}}$ is set as the product of the peak phosphorus density and the effective implantation depth. Table 4 lists the derived electrical parameters at different implantation depths.

### Table 4

<table>
<thead>
<tr>
<th>Implantation depth (µm)</th>
<th>$X_{\text{eff}}$ (µm)</th>
<th>$Q_{\text{eff}}$ (C cm$^{-2}$)</th>
<th>$V_{\text{dsatc}}$ (V)</th>
<th>$V_{\text{dsatu}}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.150</td>
<td>0.0791</td>
<td>$1.266 \times 10^{-7}$</td>
<td>7.127</td>
<td>10.658</td>
</tr>
<tr>
<td>0.200</td>
<td>0.1073</td>
<td>$1.717 \times 10^{-7}$</td>
<td>9.585</td>
<td>13.767</td>
</tr>
<tr>
<td>0.250</td>
<td>0.1367</td>
<td>$2.187 \times 10^{-7}$</td>
<td>11.978</td>
<td>16.812</td>
</tr>
<tr>
<td>0.275</td>
<td>0.1509</td>
<td>$2.414 \times 10^{-7}$</td>
<td>13.094</td>
<td>18.234</td>
</tr>
<tr>
<td>0.300</td>
<td>0.1661</td>
<td>$2.658 \times 10^{-7}$</td>
<td>14.270</td>
<td>19.737</td>
</tr>
</tbody>
</table>

4.2. Electrical model validation

Four different electrodes are set in the gate, source, drain, and substrate region and modeled as red grids to investigate the electrical output behaviors, as shown in Fig. 14(a). A voltage of 0 is applied to the gate, source, and substrate electrodes, because the fabricated transistor is a depletion-type device. Fig. 15(a) shows the channel output current $I_{\text{ds}}$ characteristics under different chan-

![Fig. 14. Simulation of the proposed fabrication process. (a) 3D LMGFET unit in the simulation. (b) Implantation concentration in the simulated device; (upleft) extracted implantation ion profile along the dotted line in the channel area. $X_{\text{eff}}$: the effective implantation depth.](image)

![Fig. 15. Channel output current $I_{\text{ds}}$ characteristics under different implantation depths. (a) Relationship between channel current $I_{\text{ds}}$ and applied drain voltage $V_{\text{ds}}$; (b) saturated channel current $I_{\text{ds}}$ and the corresponding relative errors between the calculated and simulated results. Solid lines indicate the simulated channel current, while dotted lines indicate the calculated channel current.](image)
nel implantation profiles when the applied drain voltage $V_{ds}$ increases from 0 to 20.5 V. When the implantation depth is 0.15 $\mu$m, the theoretical dotted line agrees well with the solid simulated line throughout the whole voltage range. The difference between the theoretical and simulated lines increases as the implantation depth increases. More specifically, the calculated current is smaller than that of the simulation for a low drain voltage, indicating that the proposed model is conservative in the non-saturation region. This characteristic is associated with the errors from the implantation approximation. However, the saturation region exhibiting the maximum controllable measuring sensitivity is the focus of this research, in which the theoretical calculation and simulations are in excellent accordance for all implantation depths. The calculated channel current is compared with the simulated one at the saturated voltages $V_{ds}$ and $V_{dsu}$; their relative errors are all less than 2% and are shown in Fig. 15(b).

The theoretical model is validated using the experimental data from Ref. [24] and is compared with the literature-adopted model, which assumes a constant effective gate capacitance in the uncovered channel area $C_{effu}$ and utilizes a regulation parameter for estimating the modulation effects. The experimental parameters extracted from Ref. [24] are listed in Table 5. In this study, the effective gate capacitance in the uncovered channel area $C_{effu}$ is constant and derived from the covered width $W_{chc}$ of 18 $\mu$m. In fact, $C_{effu}$ should increase with the increase in $W_{chc}$, as discussed in Section 2. Fig. 16 provides a comparison of the calculated channel current from the proposed model and the model in Ref. [24]. The two models show similar accuracy for 18 $\mu$m $W_{chc}$. The proposed model presents a close estimation for the outputs under the covered channel widths $W_{chc}$ of 0 and 60 $\mu$m. The largest relative error of the proposed model is 1.51% for a $W_{chc}$ of 0 and 2.63% for a $W_{chc}$ of 60 $\mu$m. However, those of the improved model are 6.64% and 5.84%, respectively. Therefore, the proposed model is more accurate than the previous model for LMGFET performance analysis.

### 4.3. Discussion of sensor performance

For sensor performance evaluation, the output channel current of the proposed sensor is obtained at different gate positions. Fig. 17 presents the saturated channel currents $I_{dsatc}$ and $I_{dsatu}$ of the simulations and calculation for an implantation depth of 0.275 $\mu$m. The saturated voltages $V_{dsatc}$ and $V_{dsatu}$ are set to 10.2 and 12.1 V, respectively, which are the lowest values during sensor operation. The relative error between the theoretical and simulated saturated currents is 3.88% and 5.64% at 0 $\mu$m $W_{chc}$. The mismatch under the condition of a small covered channel width mainly results from the estimation error of the capacitance expression (Eq. (2)). The relative error becomes less than 3.80% for $W_{chc} > 1$ $\mu$m. The sensitivity of the proposed device is 8.39 and 9.12 $\mu$A $\mu$m$^{-1} \cdot$V$^{-1}$ for the saturated voltages $V_{dsatc}$ and $V_{dsatu}$, respectively. Due to the low stiffness of the SU-8 movable structure, the force sensitivity of the proposed LMGFET sensor is 4.65 $\mu$A $\mu$m$^{-1} \cdot$V$^{-1}$, which is lower than that of our previous VMGFET device, which had a value of 12.53 $\mu$A $\mu$m$^{-1} \cdot$V$^{-1}$ [25]. Nevertheless, it is much higher than those of previous VMGFET devices with values of 3.24 [22] and 0.05 $\mu$A $\mu$m$^{-1} \cdot$V$^{-1}$ [23], and higher than that of a reported LMGFET device with a value of 0.01 $\mu$A $\mu$m$^{-1} \cdot$V$^{-1}$ [24]. The nonlinearity experiences a slight fluctuation because the transistor in either the covered channel area or the uncovered area disappears when the

### Table 5

Experimental parameters of the fabricated LMGFET device [24].

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length of channel $L_A$</td>
<td>30 $\mu$m</td>
</tr>
<tr>
<td>Total channel width $W_{ch} = W_{chc} + W_{chu}$</td>
<td>60 $\mu$m</td>
</tr>
<tr>
<td>Studied covered channel width $W_{chc}$</td>
<td>0, 18, 60 $\mu$m</td>
</tr>
<tr>
<td>Gate oxide thickness $t_{ox}$</td>
<td>27 nm</td>
</tr>
<tr>
<td>Effective charge density $Q_{eff}$</td>
<td>$1 \times 10^{11}$ cm$^{-2}$</td>
</tr>
<tr>
<td>Work function difference $\phi_{MS}$</td>
<td>-0.30 V</td>
</tr>
<tr>
<td>Effective gate oxide capacitance in covered area $C_{eff}$</td>
<td>$1.55 \times 10^{-6}$ F cm$^{-2}$</td>
</tr>
</tbody>
</table>

---

Fig. 16. Theoretical calculation and experimental measurement of channel current $I_{ds}$: (a) Gate fully uncovers the channel area, $W_{chu} = 0$ $\mu$m; (b) gate partially covers the channel area, $W_{chc} = 18$ $\mu$m; (c) gate fully covers the channel area, $W_{chc} = 60$ $\mu$m.
channel is fully covered or exposed. The nonlinearity approaches 0.19% and 0.78% for a $W_{\text{ch}}$ ranging from 2.5 to 17.5 $\mu$m and from 1 to 19 $\mu$m, respectively, which is much less than that of existing MGFET devices. The measurement range of the proposed sensor is $\pm5.10$ $\mu$N, which is relatively less than that of the LMGFET device in Ref. [24] but much larger than those of VMGFET devices [22,23,25].

To evaluate the overall sensing performance, the product of the sensitivity, linearity, and measurement range is calculated as a merit factor, as shown in Table 6 [22–25]. The proposed sensor exhibits the largest merit factor of 47.07 mA among existing MGFET devices, indicating that a delicate tradeoff has been made between high sensing accuracy and a large measurement range for the proposed sensor. All these characteristics make the proposed sensor a suitable choice for the measurement of ultralow forces below the nano-newton level, especially for biomedical applications requiring a large measurement range, such as cell deformation squeezing and cellular membrane penetration.

5. Conclusions

In this paper, an LMGFET micro force sensor was proposed and comprehensively analyzed. The electrical behavior of the small LMGFET unit was theoretically modeled into two individual parts and tested with simulations and experimental data. The proposed sensor exhibited improved accuracy and capability for device performance evaluation before mass fabrication. A novel sandwich structure containing a gold gate array layer and two covered SU-8 photoresist layers was developed by decoupling multiple gate arrays and using a dual-differential sensing configuration. The output current under cross-axis loadings was considerably suppressed. The electrical and structural parameters of LMGFET devices were fully analyzed in order to optimize the sensor performance, and a practicable fabrication process was developed and simulated. The proposed sensor exhibits considerably high sensitivity, linearity, and a large measurement range, making it a versatile sensing tool for biomedical micromanipulation tasks.

Acknowledgments

This work is supported in part by the National Natural Science Foundation of China (52105589 and U1909221), in part by the China Postdoctoral Science Foundation (2021M692590), in part by the Beijing Advanced Innovation Center for Intelligent Robots and Systems (2019RS08), in part by the Fundamental Research Funds for the Central Universities (China) (xyy012021009), and in part by the State Key Laboratory of Robotics and Systems (HT) (SKLRS2021KF17).

Compliance with ethics guidelines

Wendi Gao, Zhixia Qiao, Xiangguang Han, Xiaozhang Wang, Adnan Shakoor, Cunlang Liu, Dejiang Lu, Ping Yang, Libo Zhao, Yonglu Wang, Jiuhong Wang, Zhuangde Jiang, and Dong Sun declare that they have no conflict of interest or financial conflicts to disclose.

References


Table 6 Performance comparison with existing MGFET devices.

<table>
<thead>
<tr>
<th></th>
<th>Sensitivity (µA/nN)</th>
<th>Nonlinearity (%)</th>
<th>Deformation range (µm)</th>
<th>Measurement range (µN)</th>
<th>Merit factor (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>4.65</td>
<td>0.78</td>
<td>±1.00</td>
<td>±5.10</td>
<td>47.07</td>
</tr>
<tr>
<td>LMGFET [24]</td>
<td>0.01</td>
<td>7.28</td>
<td>±30.00</td>
<td>±14.50</td>
<td>0.32</td>
</tr>
<tr>
<td>VMGFET [25]</td>
<td>12.53</td>
<td>1.35</td>
<td>0.3</td>
<td>0.42</td>
<td>5.24</td>
</tr>
<tr>
<td>VMGFET [22]</td>
<td>3.24</td>
<td>11.12</td>
<td>0.2</td>
<td>0.12</td>
<td>0.35</td>
</tr>
<tr>
<td>VMGFET [23]</td>
<td>0.05</td>
<td>17.75</td>
<td>1.0</td>
<td>Na</td>
<td>Na</td>
</tr>
</tbody>
</table>

Na: not available.

* Sensitivity is unified into the same unit.