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MoS_2 Transistors with Low Schottky Barrier Contact by Optimizing the Interfacial Layer Thickness

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Abstract: Molybdenum disulfide (MoS_2) has attracted great attention from researchers because of its large band gap, good mechanical toughness and stable physical properties; it has become the ideal material for the next-generation optoelectronic devices. However, the large Schottky barrier height (Φ_B) and contact resistance are obstacles hampering the fabrication of high-power MoS_2 transistors. The electronic transport characteristics of MoS_2 transistors with two different contact structures are investigated in detail, including a copper (Cu) metal–MoS_2 channel and copper (Cu) metal–TiO_2-MoS_2 channel. Contact optimization is conducted by adjusting the thickness of the TiO_2 interlayer between the metal and MoS_2. The metal-interlayer-semiconductor (MIS) structure with a 1.5 nm thick TiO_2 layer has a smaller Schottky barrier of 22 meV. The results provide insights into the engineering of MIS contacts and interfaces to improve transistor characteristics.

Keywords: MoS_2; TiO_2; Schottky barrier; contact resistance

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1. Introduction

Two-dimensional (2D) layered materials have special properties, such as atomic-level thickness and a lack of dangling bonds on the surface. Therefore, nanodevices based on two-dimensional materials possess excellent electrical properties, such as high electron mobility and high on-off ratios. Hence, two-dimensional materials show unique application prospects in electronic devices [1–7]. Among the various 2D materials, graphene exhibits extraordinary linear dispersion for charge carriers and possesses other unique physical properties due to the ultra-thin atomic layer thickness [8,9]. The conduction and valence bands of graphene are symmetrical about the Dirac point and its energy bandgap is almost zero; this makes it difficult for graphene-based field effect transistors (FETs) to show the on-off state in devices.

Molybdenum disulfide is a typical multi-layer transition metal chalcogenide, which is composed of sulfur–molybdenum atoms bound by covalent bonds and stacked vertically in layers. The layers interact with each other through weak van der Waals forces. Compared with graphene, molybdenum disulfide is a widely used 2D material with a bandgap of 1.8 eV for the monolayer structure and 1.2 eV for the bulk materials [10,11]. The bandgap of molybdenum sulfide increases with a decreasing number of layers, and the FET based on molybdenum disulfide may be more suitable for logic circuits. Theoretically, FETs based on MoS_2 have superior room-temperature carrier mobility (410 $cm^2\ V^{-1}\ s^{-1}$) [12] and a high on/off ratio (>10^8) [13]. However, MoS_2 FETs with these excellent characteristics have yet to be realized by experiments. One key factor affecting the low carrier mobility

is the metal–MoS_2 contact and interface. Fermi level pinning leads to a large barrier height at the metal–MoS_2 contact, consequently increasing the contact resistance (R_c) at the interface [14]. Metal electrodes with different work functions have been used to improve the contact; however, when molybdenum disulfide is in contact with the metal electrode, the pinning effect of the Fermi surface changes the effects and the contact metal is very weak. Various ways to reduce the contact resistance of MoS_2 FETs have been reported. For example, H. Du et al. constructed MoS_2–graphene heterojunction FETs using single/bi-layer graphene as contact electrodes to improve the contact interface [15]. Compared to the bilayer graphene electrode, the device has better electron transport properties and higher mobility due to the better gate control capability of the single layer graphene. However, it requires the use of complex transfer techniques and is not conducive to large-scale production. Y. Du et al. prepared polyethyleneimine-doped MoS_2 FETs with reduced contact resistance and improved field-effect mobility [16]. Owing to the strong electronic doping of polyethyleneimine molecules, the mobility increases from 20.4 to 32.7 $cm^2\ V^{-1}\ s^{-1}$. The low-work-function metal (scandium) has also been used as the contact metal to improve the contact in MoS_2 FETs to obtain a higher carrier injection [17]. The device with a scandium contact has a small Schottky barrier height of 30 eV and high mobility of 184 $cm^2\ V^{-1}\ s^{-1}$. However, the poor cyclic stability of chemical doping plagues the formation of stable contacts. Low-work-function metals are easily oxidized in air, thereby limiting commercial adoption. Recently, inserting a Fermi level unpinning layer between MoS_2 and metal electrodes to construct a MIS structure was suggested to reduce Φ_B. For example, an ultrathin interlayer, such as Ta_2O_5 or h-BN, was proposed to reduce Φ_B and R_c [18,19]. Y. Kim et al. fabricated Ti-TiO_2 interlayer–MoS_2 channel FETs by the atomic layer deposition of 2.7 nm TiO_2 to reduce the noise amplitude and contact resistance [20]. Although efforts have been made to eliminate Fermi level pinning, there have been few studies on the relationship between Fermi level unpinning and device performance.

In this work, we systematically study the above issues by modulating the thicknesses (0, 1, 1.5 and 2.2 nm) of the TiO_2 interfacial layer. The barrier height and contact resistance of different TiO_2 intercalation thicknesses are studied in detail. After inserting a 1.5 nm thick TiO_2 layer into the meta–MoS_2 interface, the MIS structure shows a reduced Φ_B of 22 meV and an R_c of 4 kΩ·μm. The electron mobility is also derived for different TiO_2 intercalation thicknesses. The mobility is closely related to the contact interface between the metal and MoS_2, and the intrinsic mobility is easily masked by the Schottky barrier at the contact interface. As a result of the improved interface, the MoS_2–TiO_2 FET shows the highest field-effect mobility of 58 $cm^2\ V^{-1}\ s^{-1}$. The barrier height and contact resistance can be controlled by the TiO_2 thickness; thus, this provides insights into the design of MIS FETs.

2. Experimental Samples and Analysis Techniques

Device Fabrication and Measurements: The multilayer MoS_2 flakes were exfoliated onto the SiO_2/Si substrate (300 nm thick SiO_2). Ti layers with various thicknesses of 0.2–1 nm were deposited on the MoS_2 surface by electron beam evaporation; and vaporizing the low melting point metal for re-oxidation, thus avoiding damage of the surface of the materials. The devices were dried in an oven for two days. As shown in Figure 1, the TiO_2 layers after oxidation were analyzed by atomic force microscopy (AFM); moreover, the TiO_2 thicknesses were determined to be 1, 1.5, 1.8, 2.2 and 2.5 nm. Methyl methacrylate (MMA) and polymethyl methacrylate (PMMA) were spin-coated on the substrate; electron beam lithography (JEOL 6510 with NPGS) was used to define the source/drain patterns. The source and drain electrodes (15/50 nm thick Cu/Au film) were formed by thermal vaporizer deposition. Acetone was used in the lift-off process to form the electrodes. Electrical characterization was conducted on the Lake Shore TTPX Probe Station and Agilent 4155C Semiconductor Parameter Analyzer in vacuum.

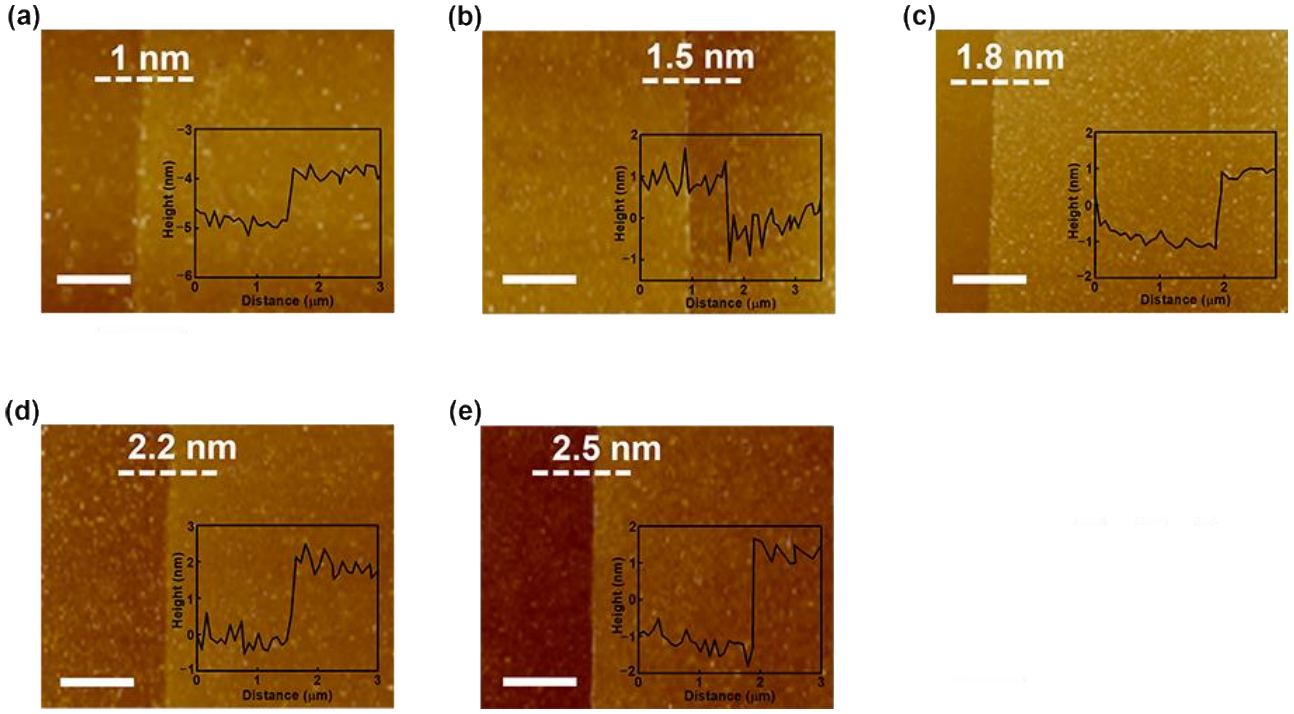

Figure 1. (**a**–**e**) AFM images of the TiO_2 interlayers with different thicknesses on the SiO_2 substrate. The thicknesses of Ti are 0.2, 0.4, 0.6, 0.8 and 1 nm; these correspond to thicknesses of TiO_2 of 1, 1.5, 1.8, 2.2 and 2.5 nm, respectively. The scale bar is 2 μm.

Characterization: The TiO_2 thickness was determined by AFM (Bruker Multimode 8) and the XPS spectra were acquired on the Thermo Fisher ESCALAB 250Xi system (Thermo Fisher Scientific, Waltham, MA, USA) with an Al K_α X-ray source. The MoS_2 flakes were analyzed by Raman scattering (RENISHAW Invia) with a 532 nm laser under ambient conditions.

3. Results and Discussion

Figure 2a displays the schematic of the MoS_2 FETs with a TiO_2 layer between the metal electrode and MoS_2 contact. Figure 3a shows the Ti 2*p* XPS spectra of TiO_2 with different thicknesses. The peaks at 458.5 eV and 464.2 eV are consistent with Ti $2p_{1/2}$ and Ti $2p_{3/2}$, respectively; with the latter being associated with Ti^{4+} [21]. When the thickness of Ti is 3 nm, the sample is not fully oxidized and the peak shows an obvious left shift; this means that part of Ti^{4+} is reduced to a low-valence Ti^{x+} species [22]. Therefore, it is important to vaporize a suitable metal thickness to obtain a high-quality interfacial layer. The Raman spectra do not change significantly after coverage with a TiO_2 layer (Figure 2b), indicating marginal lattice damage during deposition of the low melting point metal. Figure 2c,d show the band diagrams of the MS and MIS structures based on the multilayer MoS_2 FETs. According to the metal-induced gap state theory [23,24], when the metal is in contact with the semiconductor, the metal electron wave function decays exponentially into the semiconductor bandgap; this results in a high interface state density at the metal–semiconductor interface, which drives the intrinsic Fermi level to move toward the electroneutral region (Figure 2c). Inserting an ultrathin interfacial layer at the metal–semiconductor interface can prevent penetration of the metal electron wavefunction into the semiconductor; thus, this results in fewer interstitial states and unpinning the surface (Figure 2d). Another mechanism is dipole formation at the interlayer–semiconductor interface to reduce Φ_B [25,26].

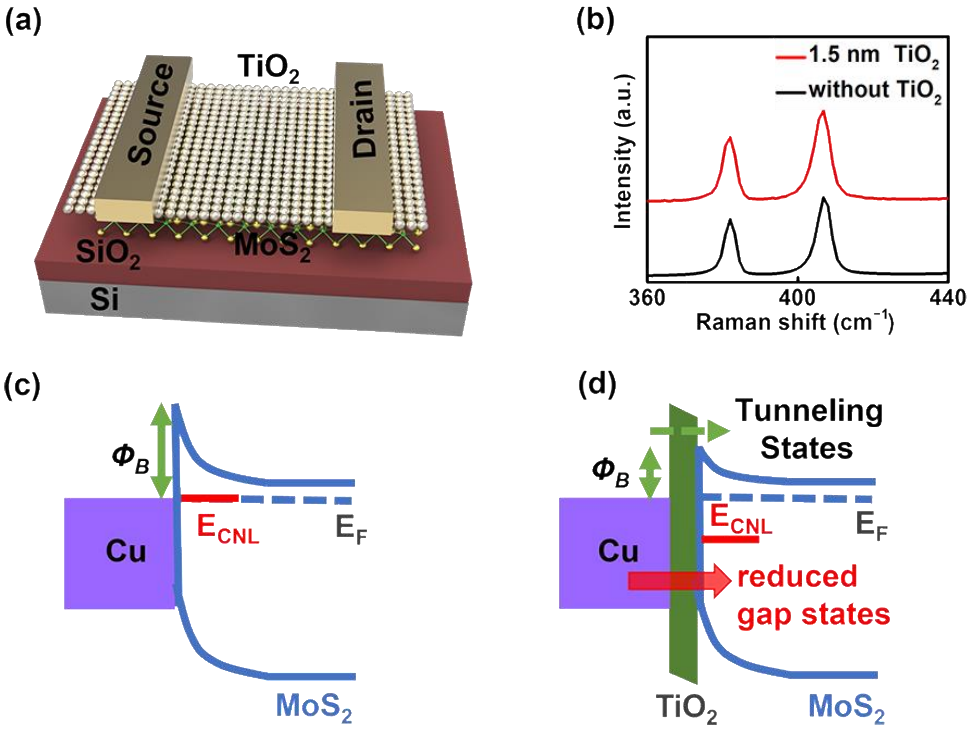

Figure 2. (**a**) Fabrication schematic of the MoS_2 FETs with a TiO_2 interlayer; (**b**) Raman scattering spectra of the multilayer MoS_2 without and with the TiO_2 layer; (**c**,**d**) band diagrams of the MS structure and MIS structure.

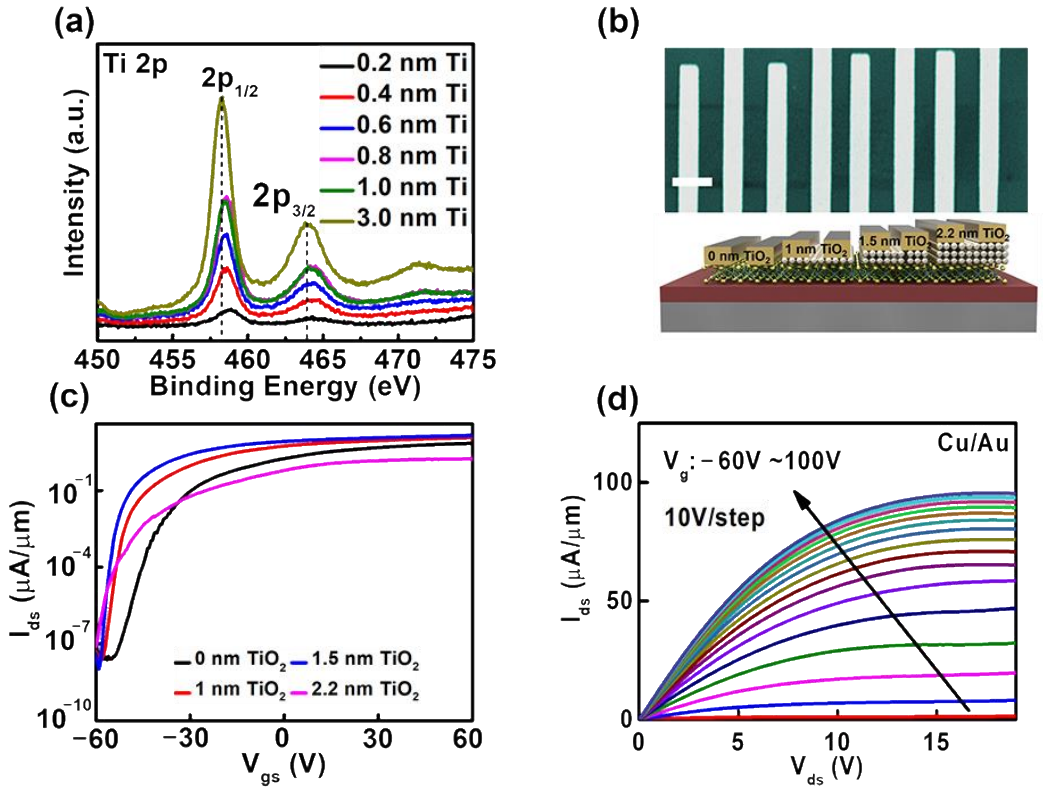

Figure 3. (**a**) Ti 2p spectra of TiO_2 with different thicknesses; (**b**) SEM image and schematic diagram of the back-gated Cu-TiO_2-MoS_2 FETs with various TiO_2 thicknesses (0, 1, 1.5 and 2.2 nm) (scale bar = 5 μm); (**c**) transfer characteristics of the devices for various TiO_2 thicknesses with L being 3 μm and V_{ds} being 1 V; (**d**) output characteristics of the Cu-TiO_2-MoS_2 FETs.

The scanning electron microscopy (SEM) image and schematic diagram of the devices with different TiO_2 interlayer thicknesses of 0, 1, 1.5 and 2.2 nm are exhibited in Figure 3b. Figure 3c shows the transfer characteristic curves of the device with various TiO_2 thicknesses. The data are acquired at a source-drain voltage (V_{ds}) of 1 V. Figure 3c shows that the source-drain current is largely dependent on the TiO_2 interlayer thickness and the device with the 1.5 nm TiO_2 interlayer shows the optimal characteristics. The increase in the drain current is mainly attributed to the reduced Schottky barrier and contact resistance. When the TiO_2 interlayer thickness is 2.2 nm, a larger tunneling resistance is obtained; in addition, the source-drain current is reduced. The field-effect mobility μ can be estimated from the transfer curve by the following relationship:

$$\mu = g_m \frac{1}{C_{ox}} \frac{L}{W} \frac{1}{V_{ds}} \quad (1)$$

where C_{ox} is the gate capacitance, L = 3 μm is the length, W is the channel width and $g_m = dI_{ds}/dV_{gs}$ is the transconductance. As the gate voltage increases, the transconductance increases to a maximum value and then saturates. The extracted field-effect mobility values for the four TiO_2 thicknesses (0, 1, 1.5 and 2.2 nm) are 27, 44, 58 and 11 $cm^2\ V^{-1}\ s^{-1}$, respectively. The mobility of the device increases gradually after insertion of the TiO_2 interface layer. When the thickness of the TiO_2 interface layer is increased to 2.2 nm, the properties of the device begin to degrade. In particular, the mobility of the device with a 1.5 nm thick TiO_2 interlayer increases by more than double compared to that before deposition of TiO_2. Figure 3d shows the output characteristic curves of the device with 1.5 nm TiO_2 thickness at different gate voltages (V_{gs}) ranging from −60 to 100 V. The device exhibits large current output and good cycling stability, further confirming that the insertion of the TiO_2 interface layer improves the contact behavior. The results show that the TiO_2 interlayer can improve the contact between the metal electrode and molybdenum disulfide. This may be because the intercalation of TiO_2 avoids bonding between sulfur in molybdenum disulfide and the electrode metal; thus, this reduces the interface state and improves the contact compared to the evaporation of the metal electrode. To further elucidate the reasons for the improvement, R_c and Φ_B are measured. The introduction of an interfacial layer at the contact reduces Φ_B and increases the tunneling resistance. A thick interfacial layer results in a large tunneling resistance, but a small current flow through the device. Therefore, it is important to deposit an appropriate interfacial layer thickness to attain the best performance.

Contact resistance, an important performance indicator for transistors, is measured by the transmission line method (TLM). The contact resistances of the samples with various TiO_2 thicknesses are shown in Figure 4. The gate voltage can adjust the carrier concentration of the molybdenum sulfide channel, thereby changing the contact resistance. $V_{g\text{-}t}$ corresponds to the gate voltage minus threshold voltage. The device with the 1.5 nm TiO_2 interlayer shows the minimum contact resistance of 4 kΩ·μm, which is smaller than the 8.2 kΩ·μm of that without the TiO_2 interlayer. As the thickness of TiO_2 is increased to 2.5 nm, R_c increases to 46 kΩ·μm and the large tunneling resistance results in poor performance. To further analyze the mechanism of R_c reduction, Φ_B is measured to study the influence of different interlayer thicknesses. The Schottky barrier height is derived by the following formula [27,28]:

$$I_{ds} = A_{2d}^{*} T^{3/2} \exp\left(\frac{q\Phi_B}{k_B T}\right)\left[1 - \exp\left(-\frac{qV_{ds}}{k_B T}\right)\right] \quad (2)$$

In this Equation (2), I_{ds} is the current, A^* is the Richardson's constant, T is the temperature, q is the electronic charge, k_B is the Boltzmann constant and V_{ds} is the drain to source voltage. The effective barrier height here is different from that of the metal–semiconductor structures due to the insertion of the interfacial layer. Because insulators are not considered in expression (2) used to determine the barrier height, the effective barrier height given here

represents the whole electronic behavior. When the gate bias is lower than the flat band voltage (V_{fb}), the device works in the thermionic emission state. The contribution of the tunneling current becomes significant when at a high gate bias ($V_{gs} > V_{fb}$) [29,30]. The slopes of these lines provide the effective Schottky barrier height, as shown in Figure 5a–f. Φ_B at a flat band voltage for the device without the TiO_2 layer is 168 meV (Figure 5a). Compared to Φ_B without the TiO_2 layer, Φ_B of the device with the lowest R_c is 22 meV for a 1.5 nm TiO_2 interfacial layer (Figure 5c). It is important that Φ_B associated with R_c can be controlled by the thicknesses of the TiO_2 layer. These results show that the metal–semiconductor contact interface is severely affected by Fermi level pinning; however, it is not greatly affected by the metal work function.

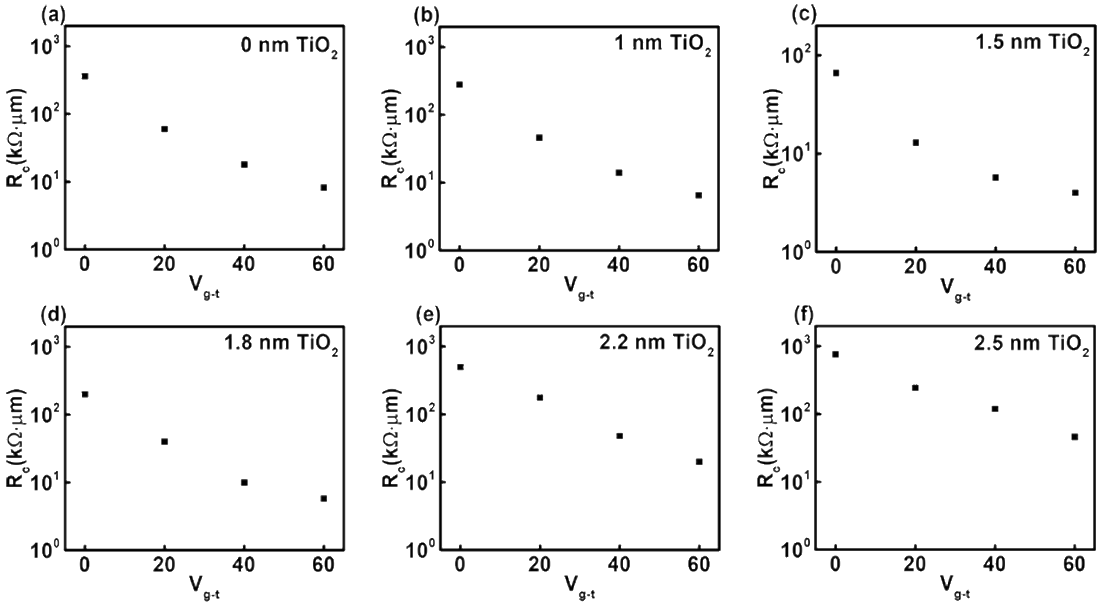

Figure 4. (**a**–**f**) Contact resistances for various TiO_2 thicknesses.

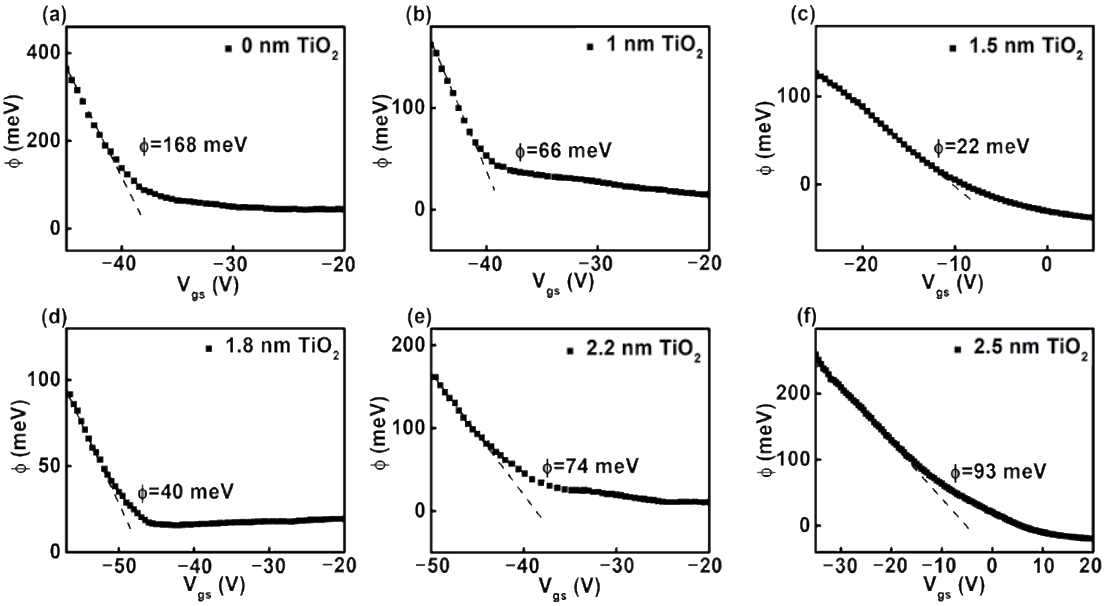

Figure 5. (**a**–**f**) Effective Schottky barrier heights as a function of gate overdrive for various TiO_2 thicknesses.

The MIS structures include two types of resistance: Schottky barrier resistance (R_{SB}) and tunneling resistance (R_T). Without an interlayer, a large Φ_B causes a large R_{SB}, which

is the main part of the entire contact resistance. By inserting a TiO_2 layer to reduce Φ_B, R_{SB} decreases accordingly. When the interfacial layer exceeds the optimal thickness, R_T dominates the contact resistance; thus, this increases the overall contact resistance. By optimizing the thickness of the interfacial layer, a trade-off between R_{SB} and R_T can be obtained. The FETs with the 1.5 nm TiO_2 layer have the minimum contact resistance, lowest Schottky barrier height and optimal properties consistent with Figure 3c. The TiO_2 interface layer has two functions: first, it obtains a reduced Schottky barrier and contact resistance in the source-drain contact area; and second, it acts as a dielectric shield and increases charge density at the TiO_2–MoS_2 interface. At the same time, the moisture and oxygen in the air are isolated; moreover, the stability of the device is improved. Using TiO_2 as an interfacial layer results in the lowest Φ_B because of the small conduction band offset between MoS_2 and TiO_2, which is more conducive to carrier injection.

4. Conclusions

The N-type MoS_2 field-effect device with good contact is fabricated by using TiO_2 as the interlayer between MoS_2 and the metal electrode. By evaporating a low melting point metal and then, performing re-oxidation, damage is avoided in the materials; in addition, the stability of the equipment is ensured. The effect of the interlayer thickness on the device characteristics is investigated systematically. The thickness of the interfacial layer plays a crucial role in the device properties. The device with a 1.5 nm thick TiO_2 as the interfacial layer shows a small Φ_B of 22 meV and a low R_c of 4 kΩ·μm. The results provide important clues to contact engineering and how to improve 2D semiconductor devices. The MIS structure is also effective in solving the contact problems and presents a potential solution for contacts in devices based on 2D materials.

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